

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J50S MLB_S

Wed Nov 16 13:50:00 2011

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

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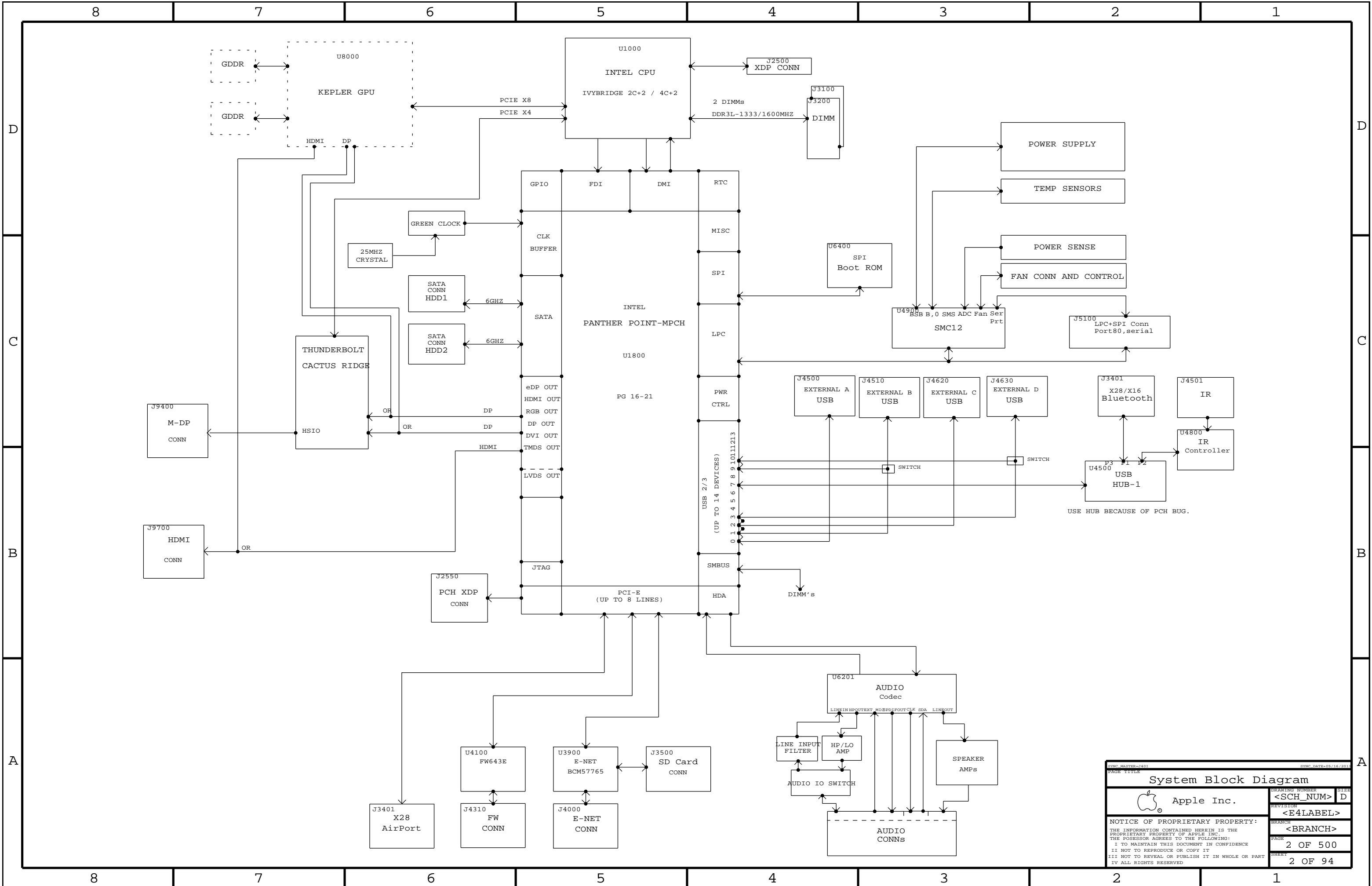
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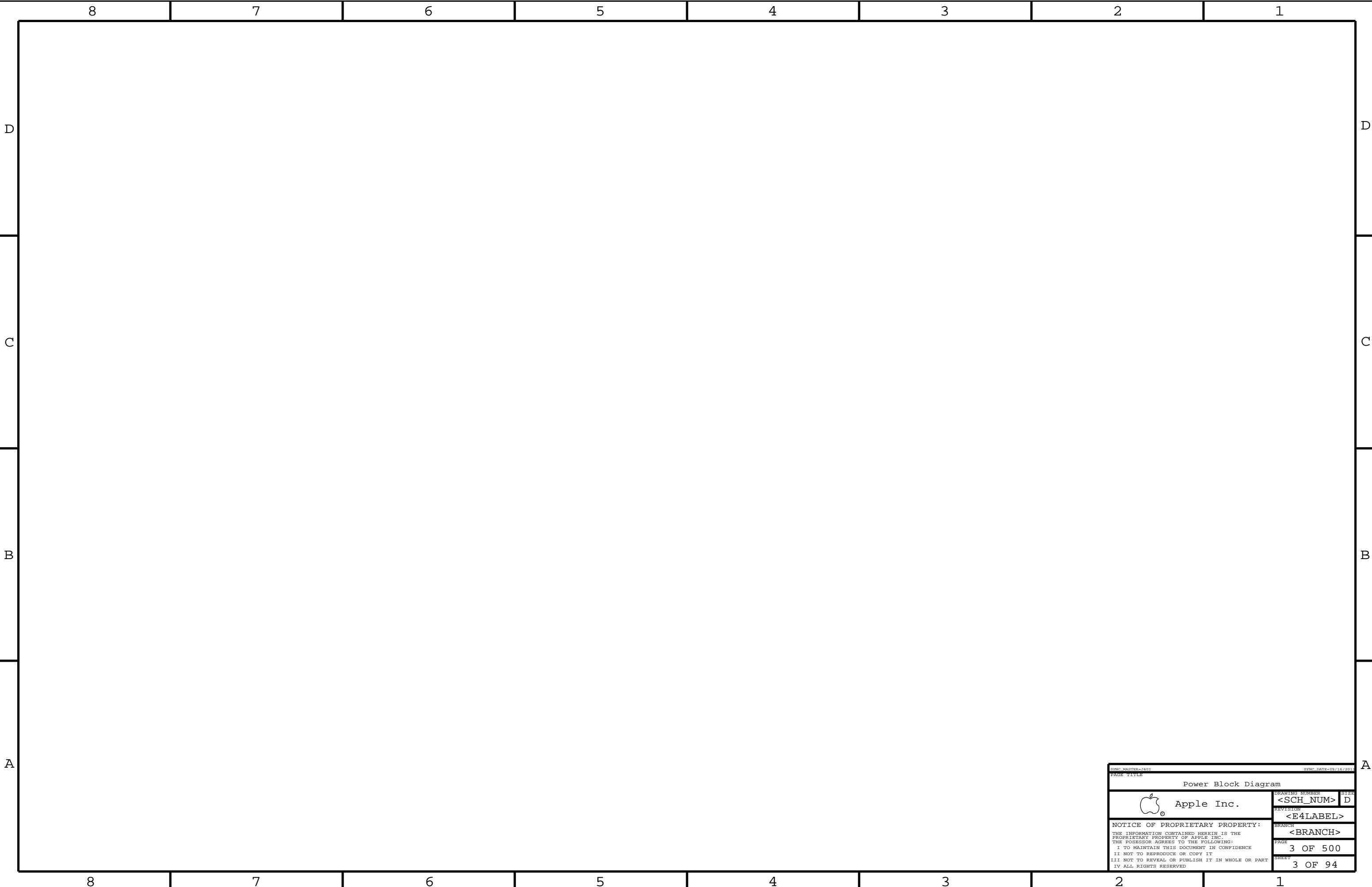
DOCUMENTS / BOARDS / ASSEMBLIES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9342	1	SCH,MLB-S,J50S	SCH		
820-3228	1	PCBF,MLB-S,J50S	MLB		
639-3211		PCBA,MLB-S,J50S			
085-4181	1	DEV LIST,MLB-S,J50S	DEV1		DEVELOPMENT_LIST

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SCH, MLB_S, J50S	
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Power Block Diagram

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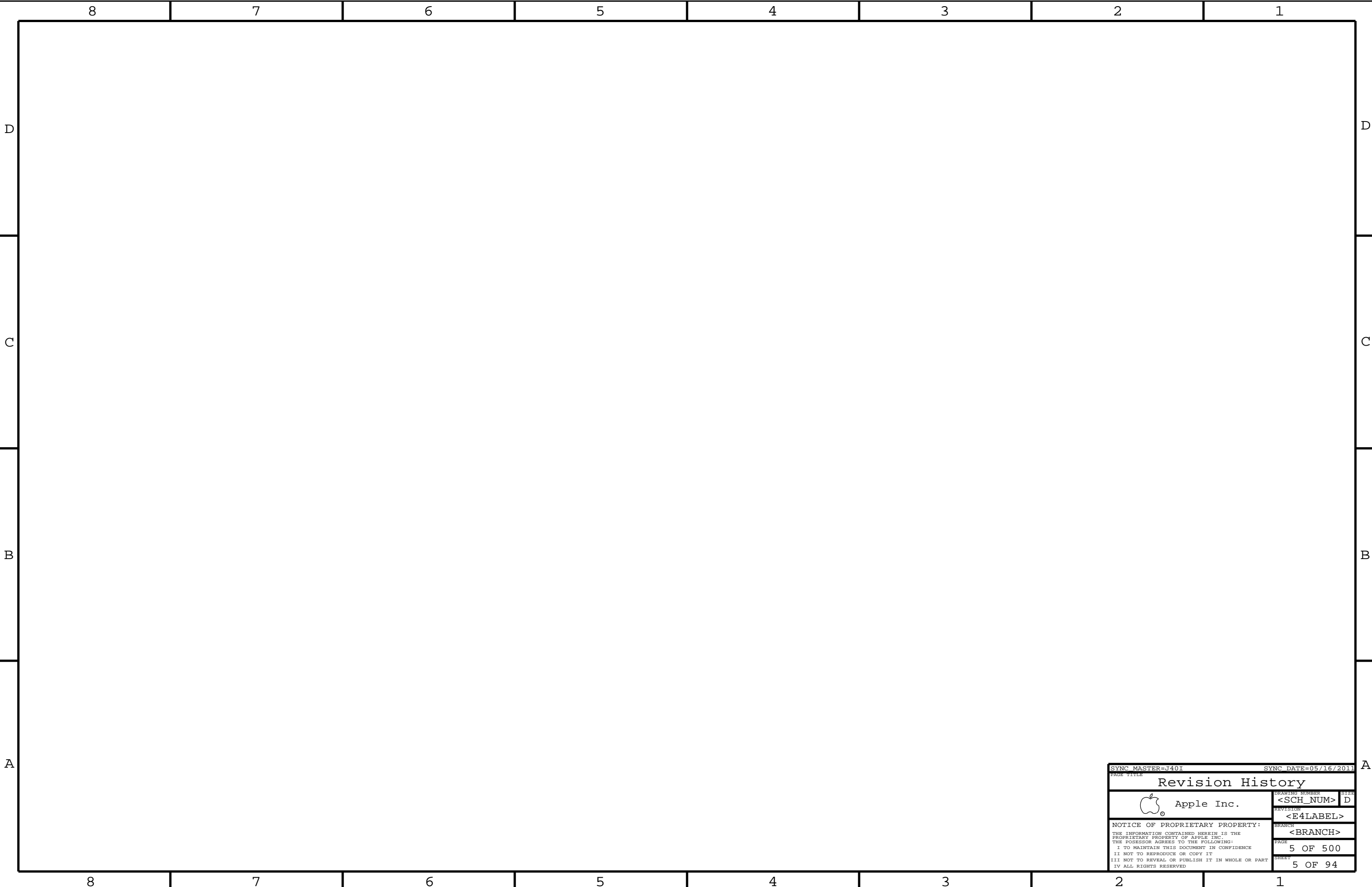
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Revision History

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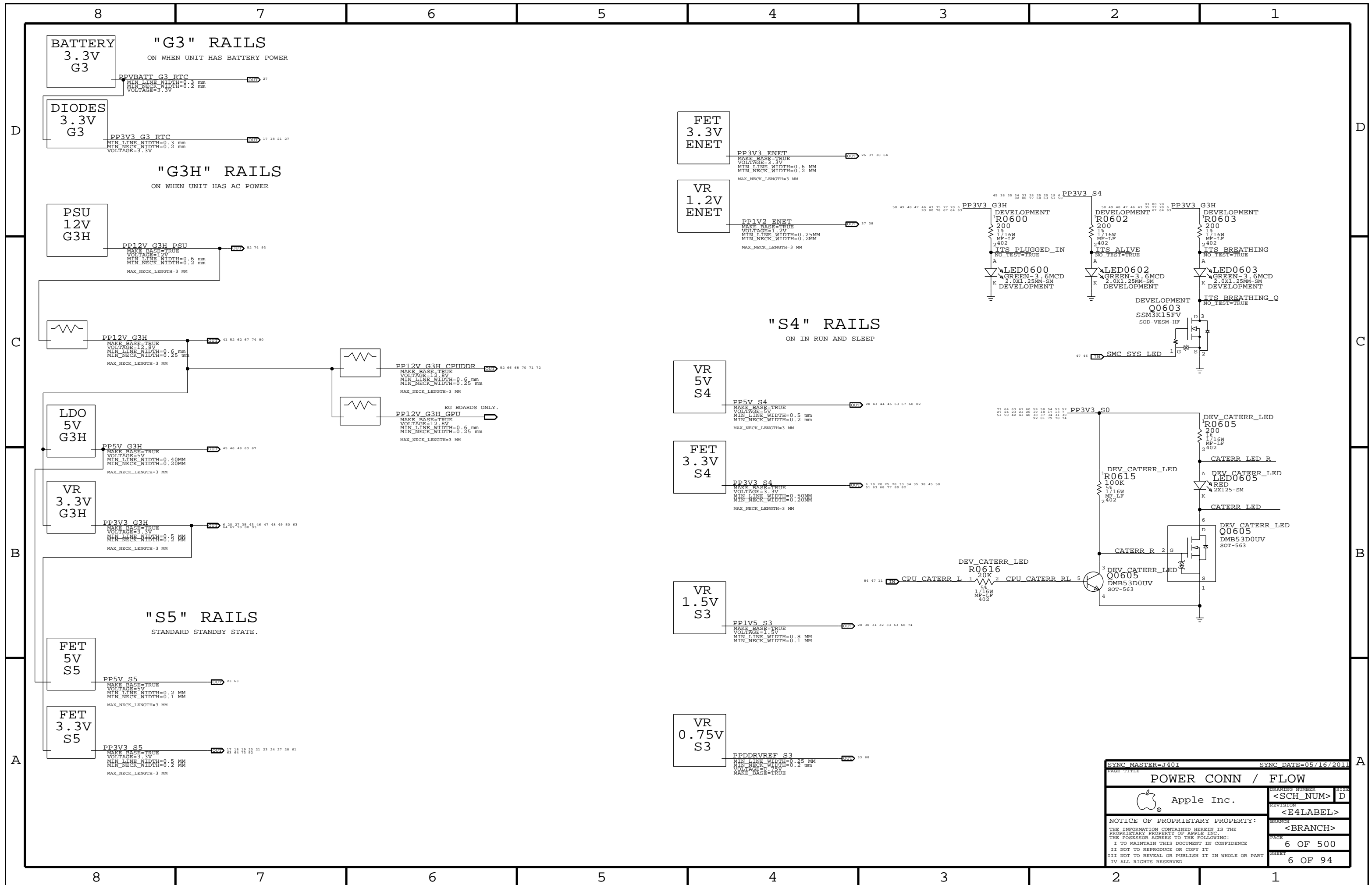
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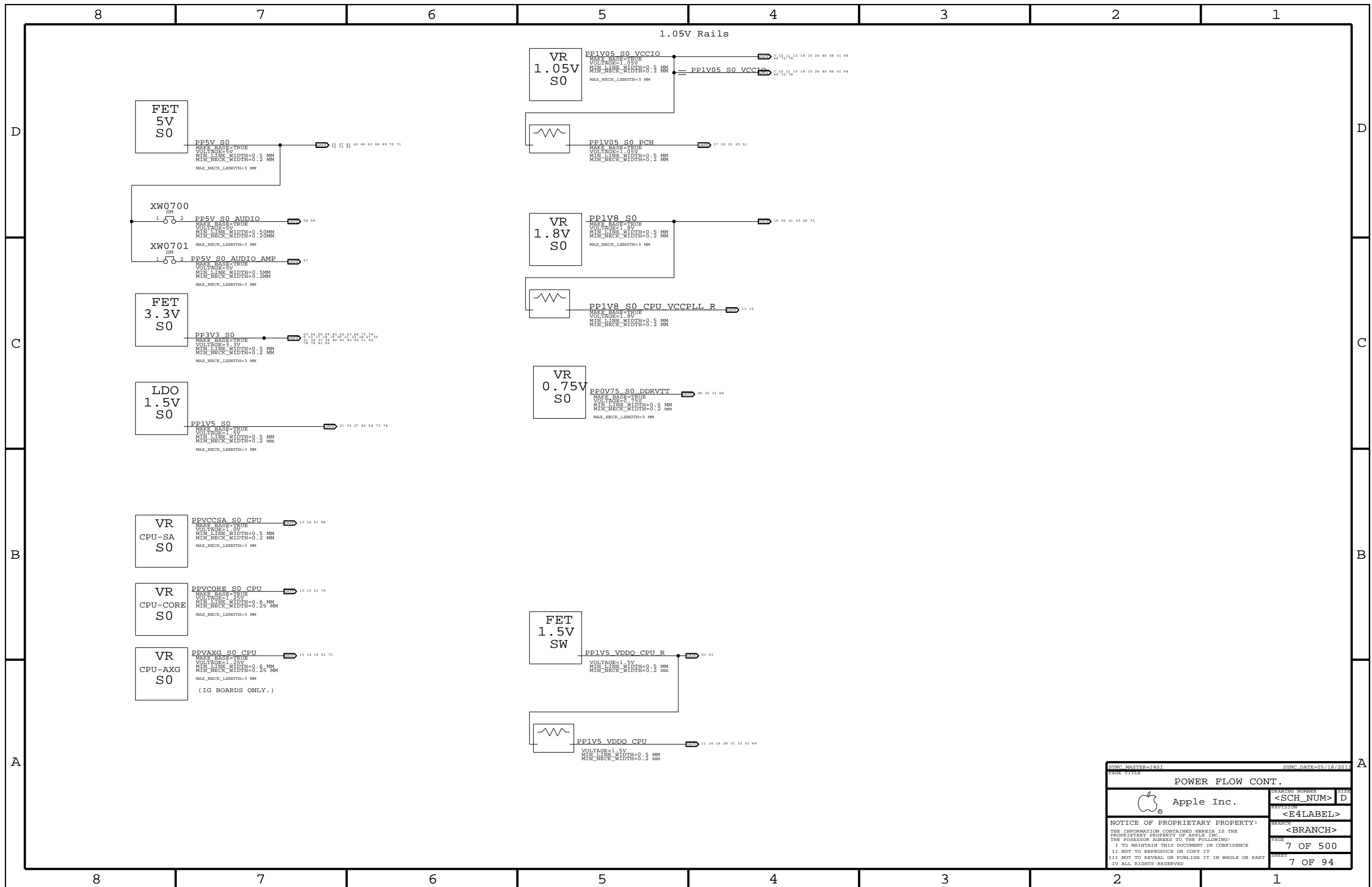
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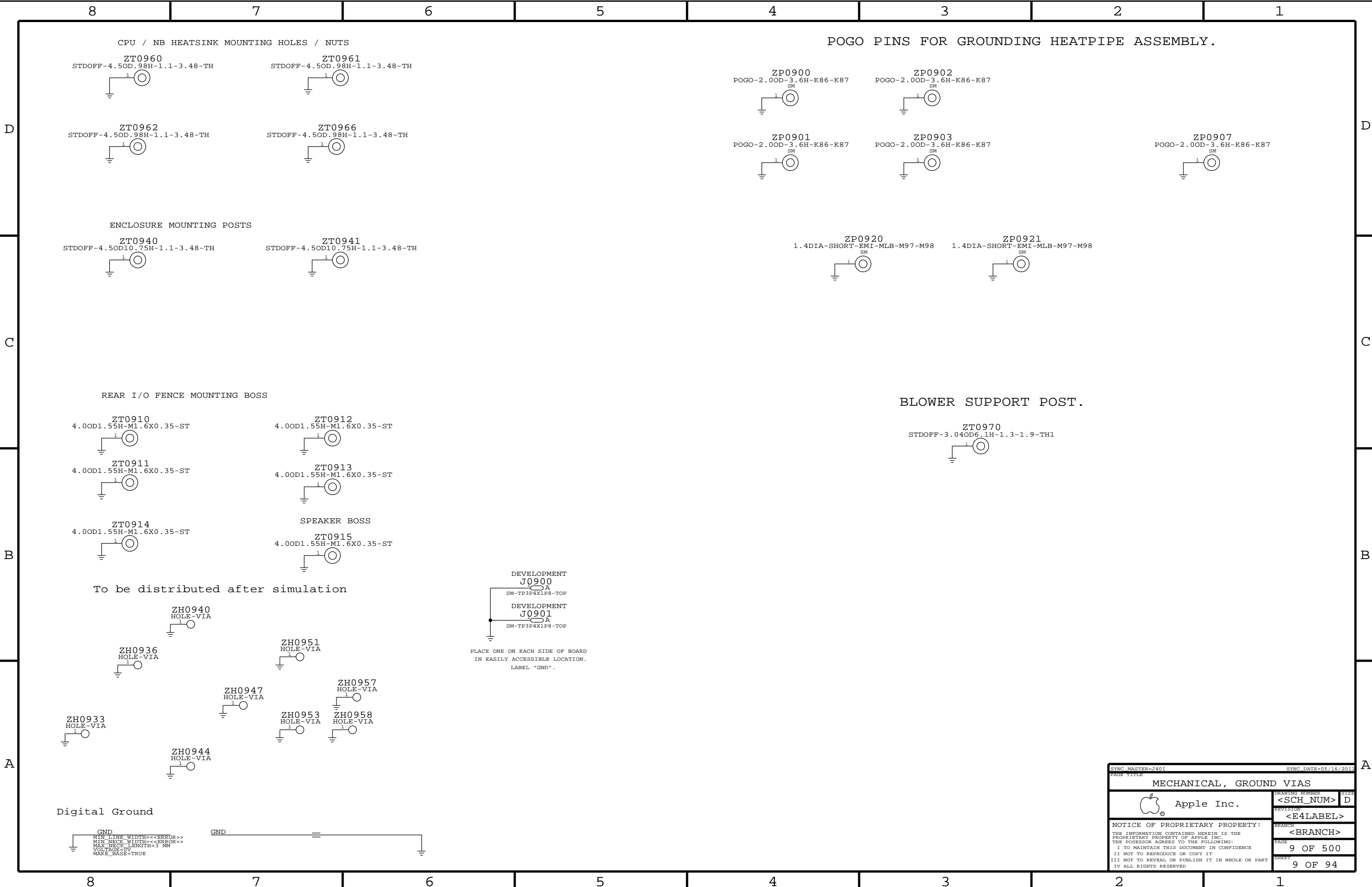
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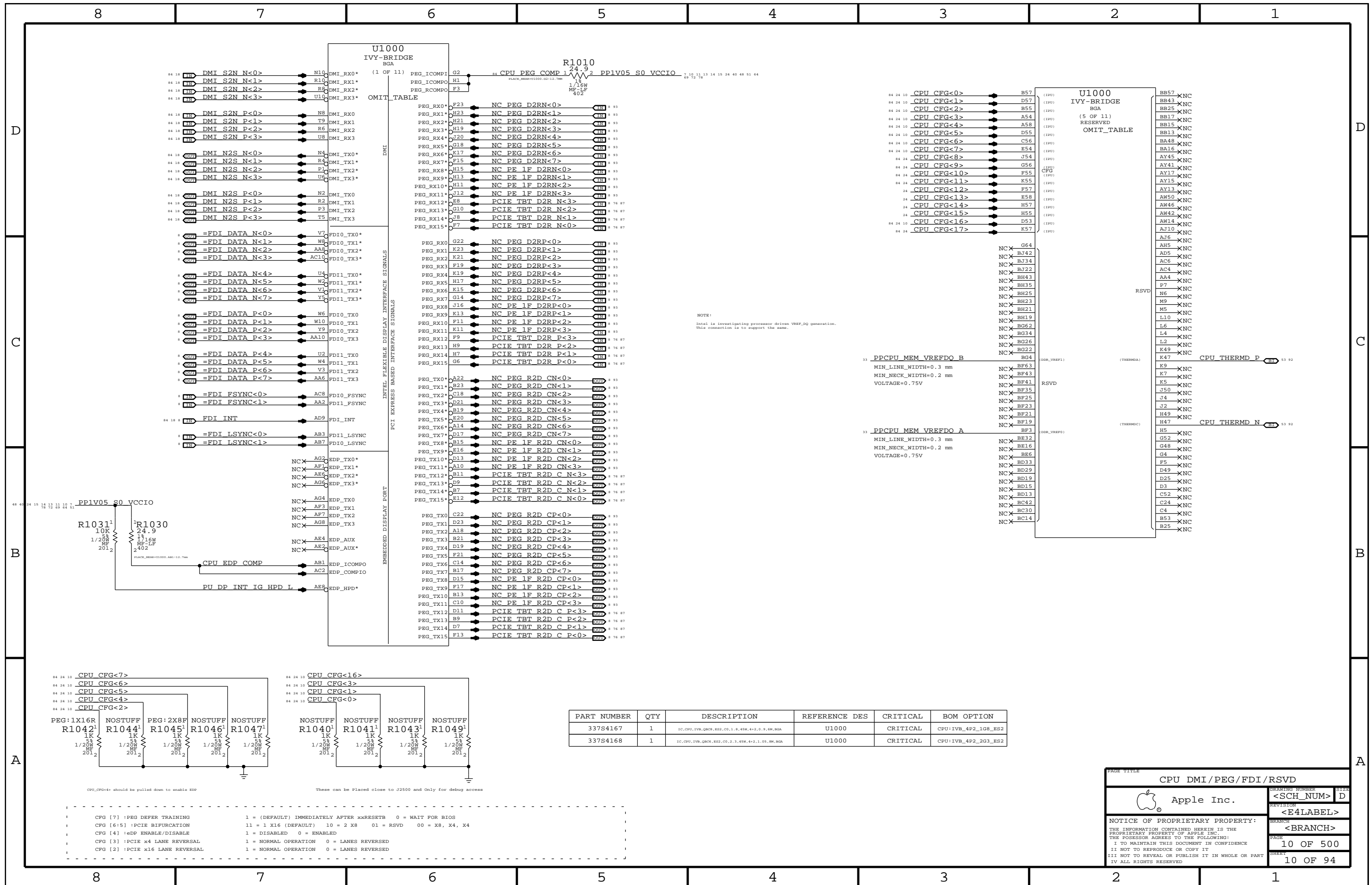


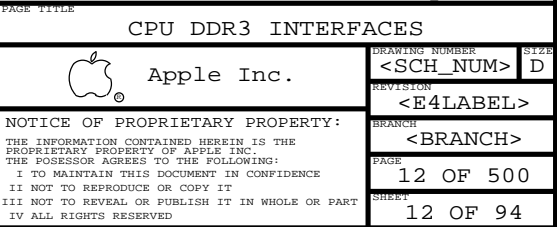
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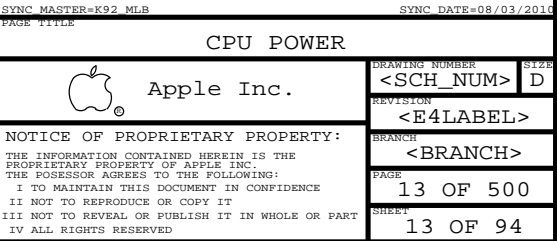


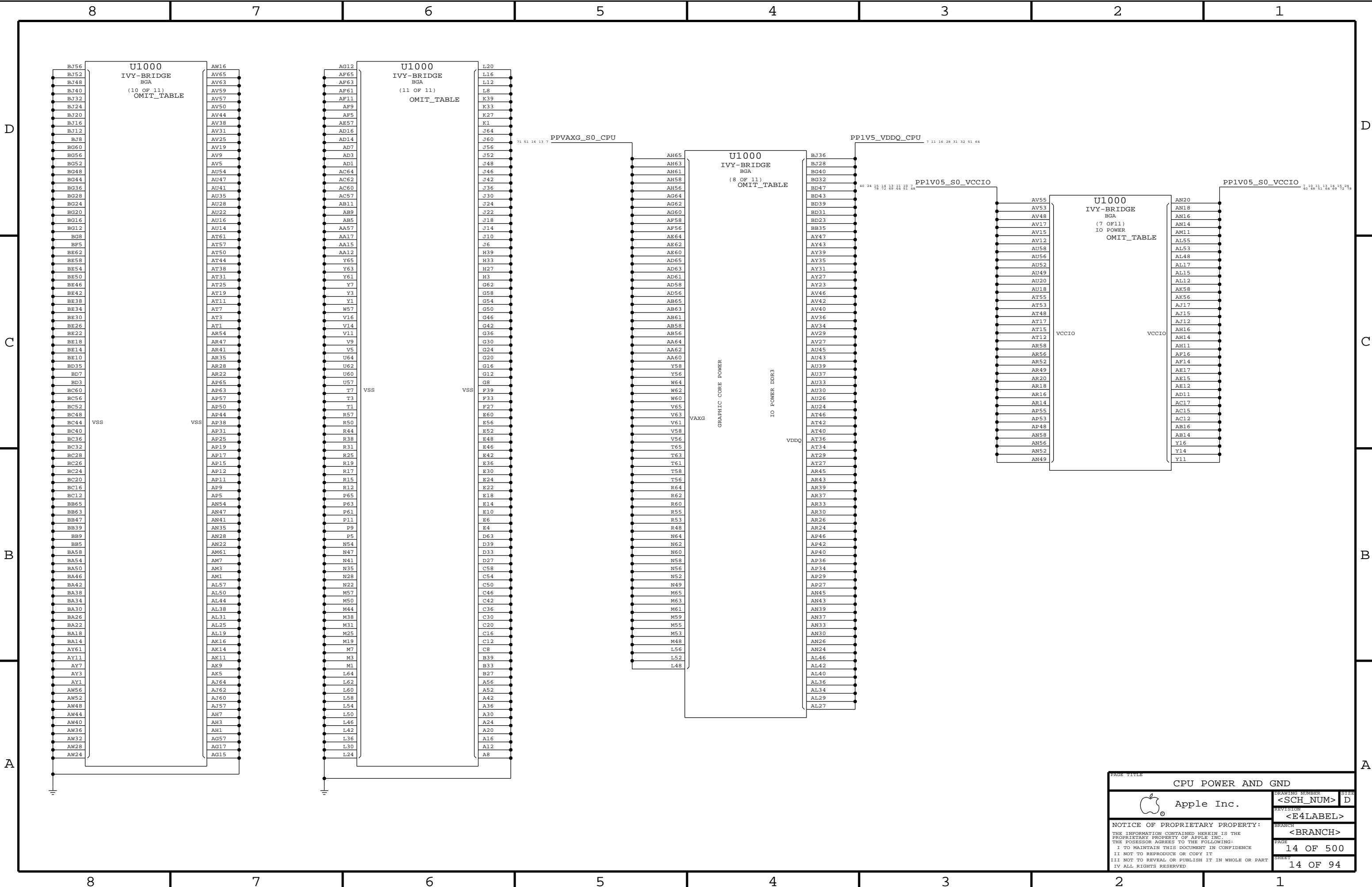
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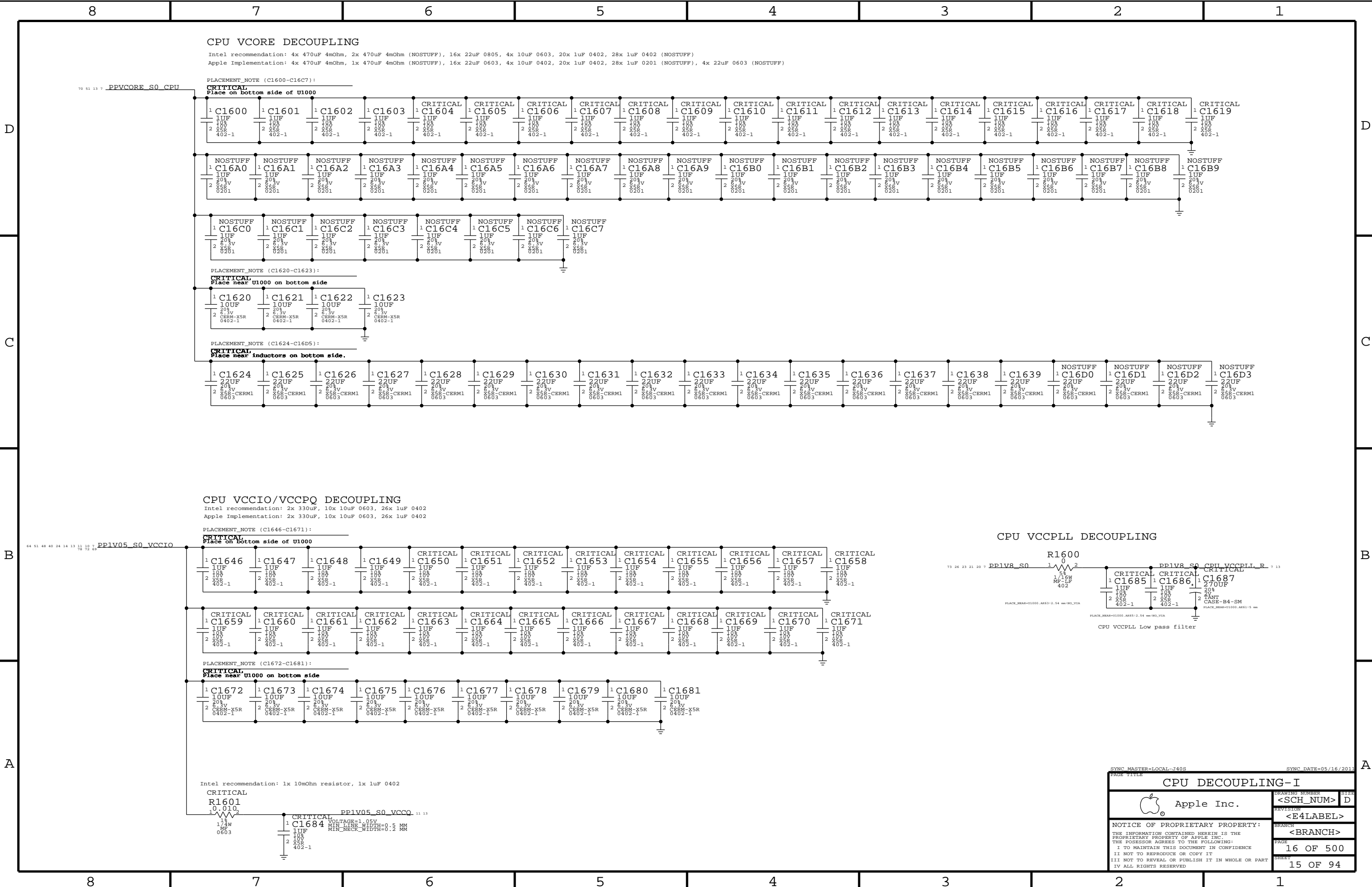


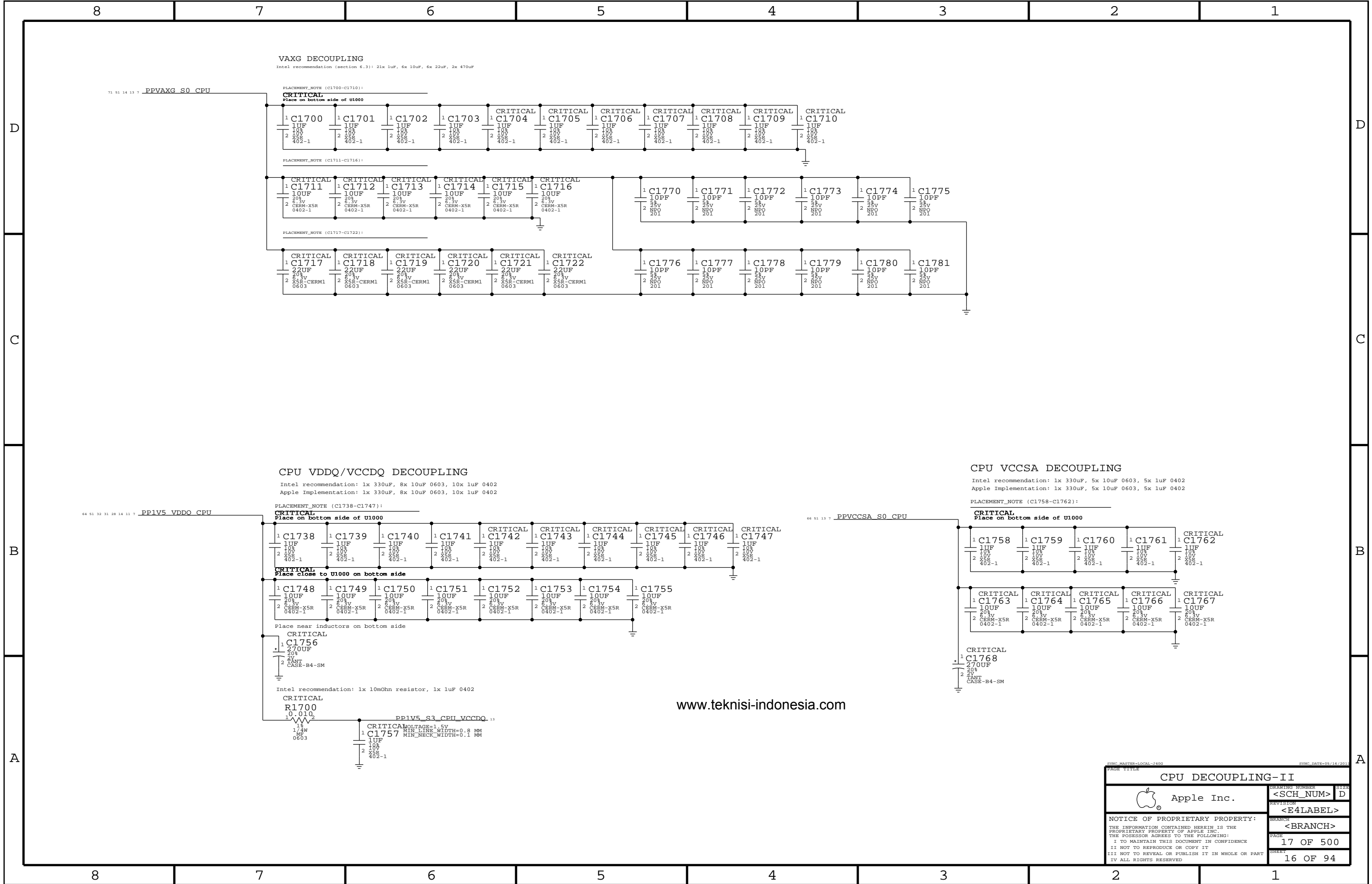


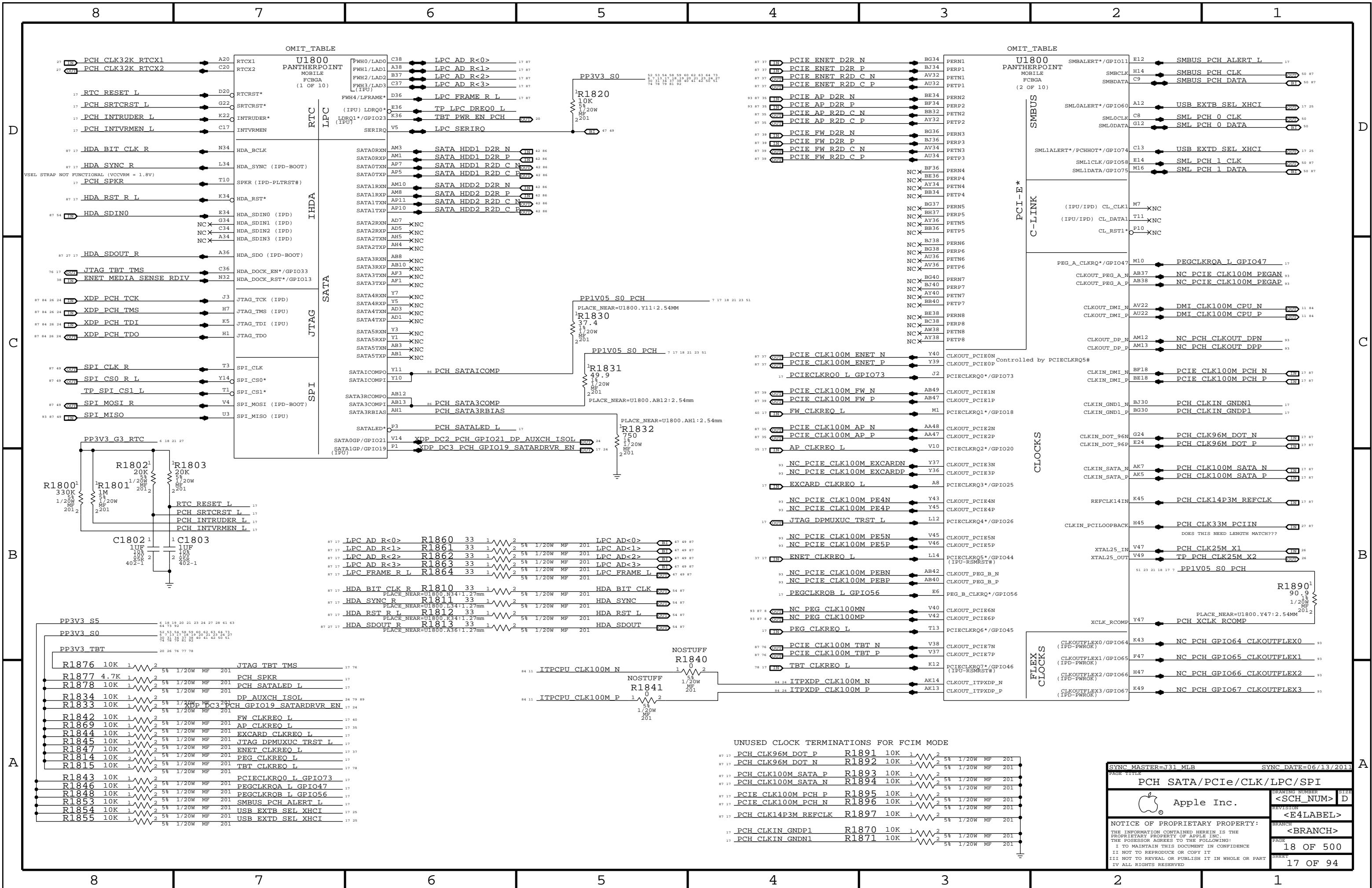


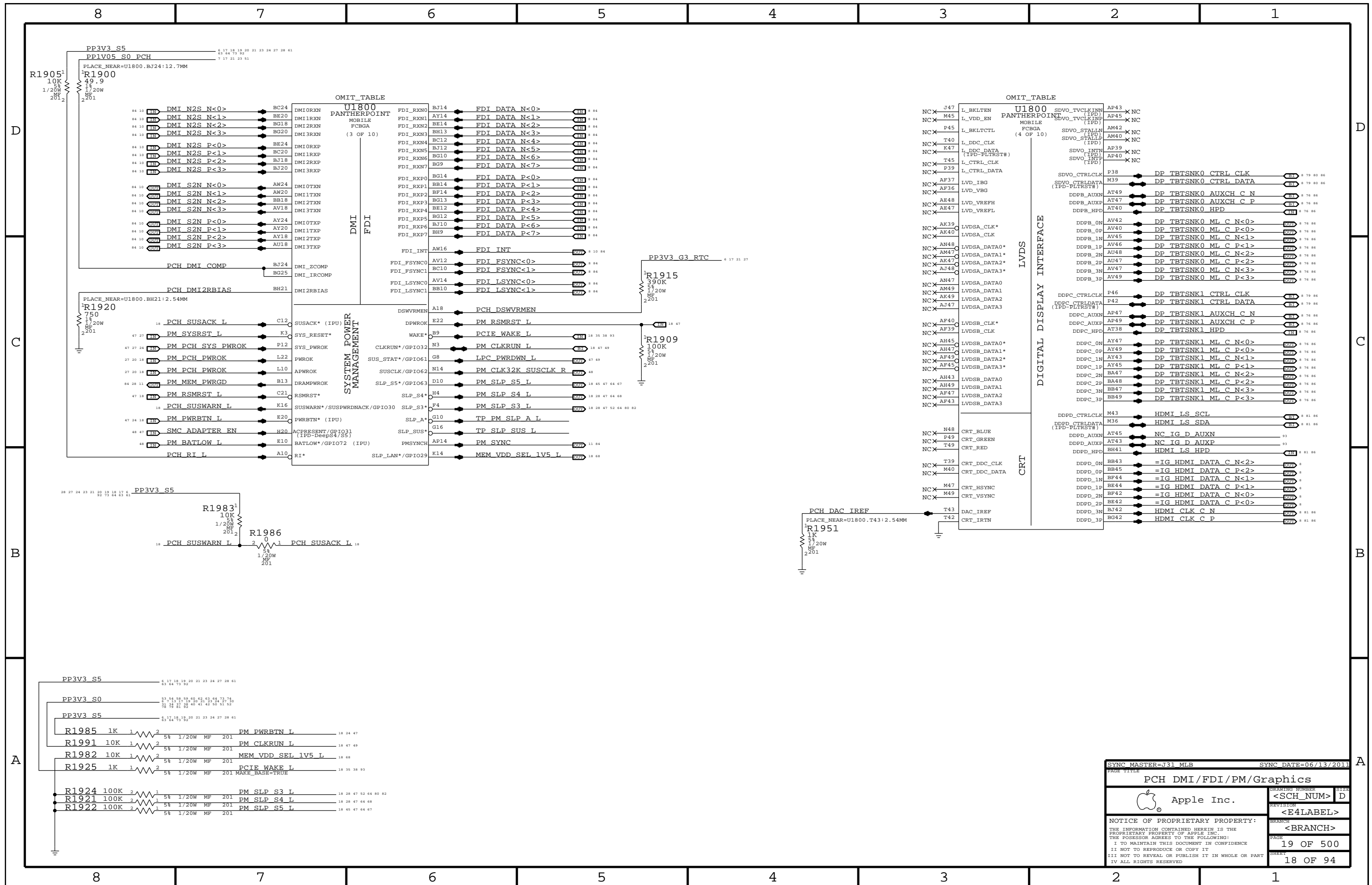


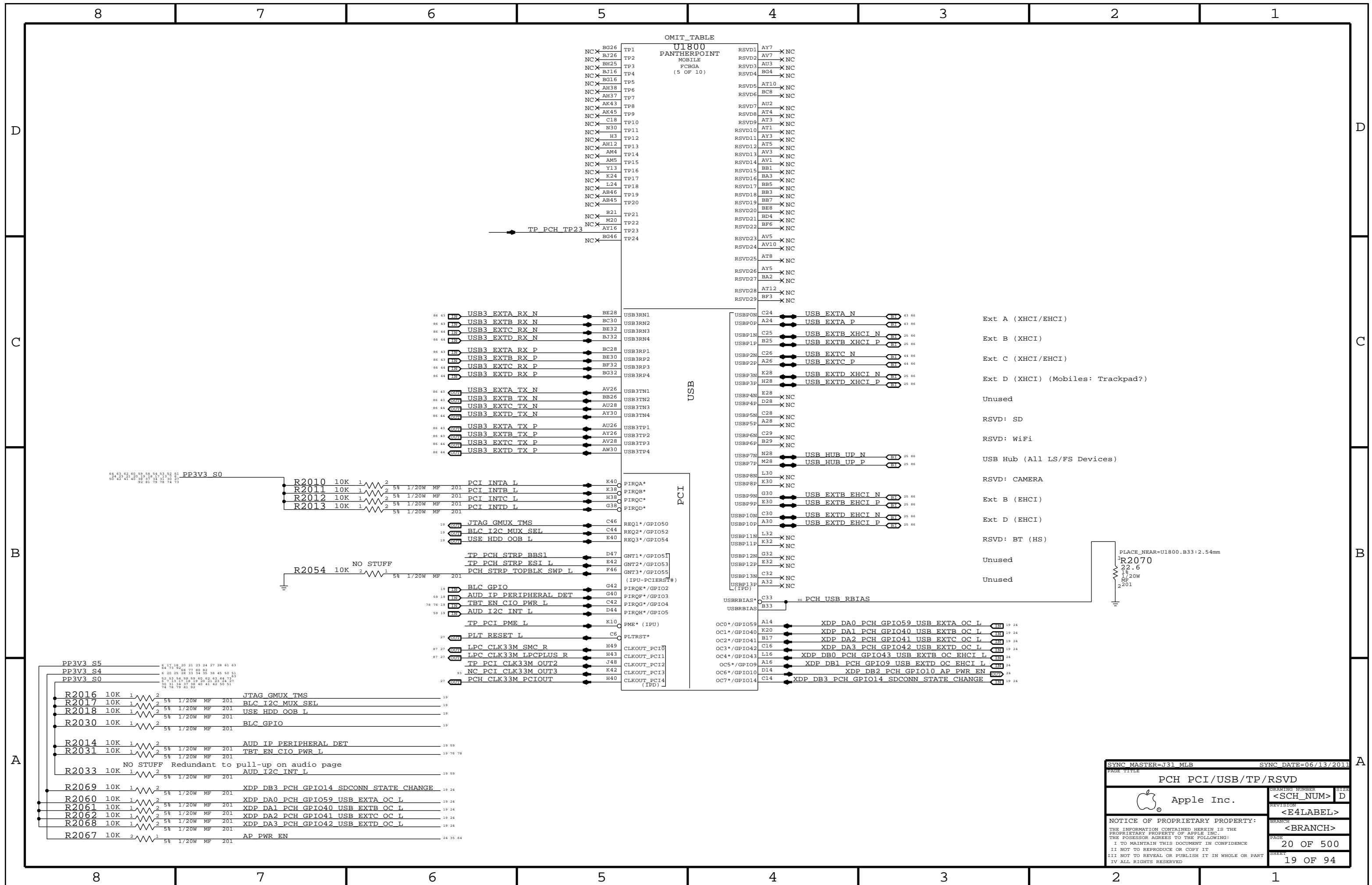




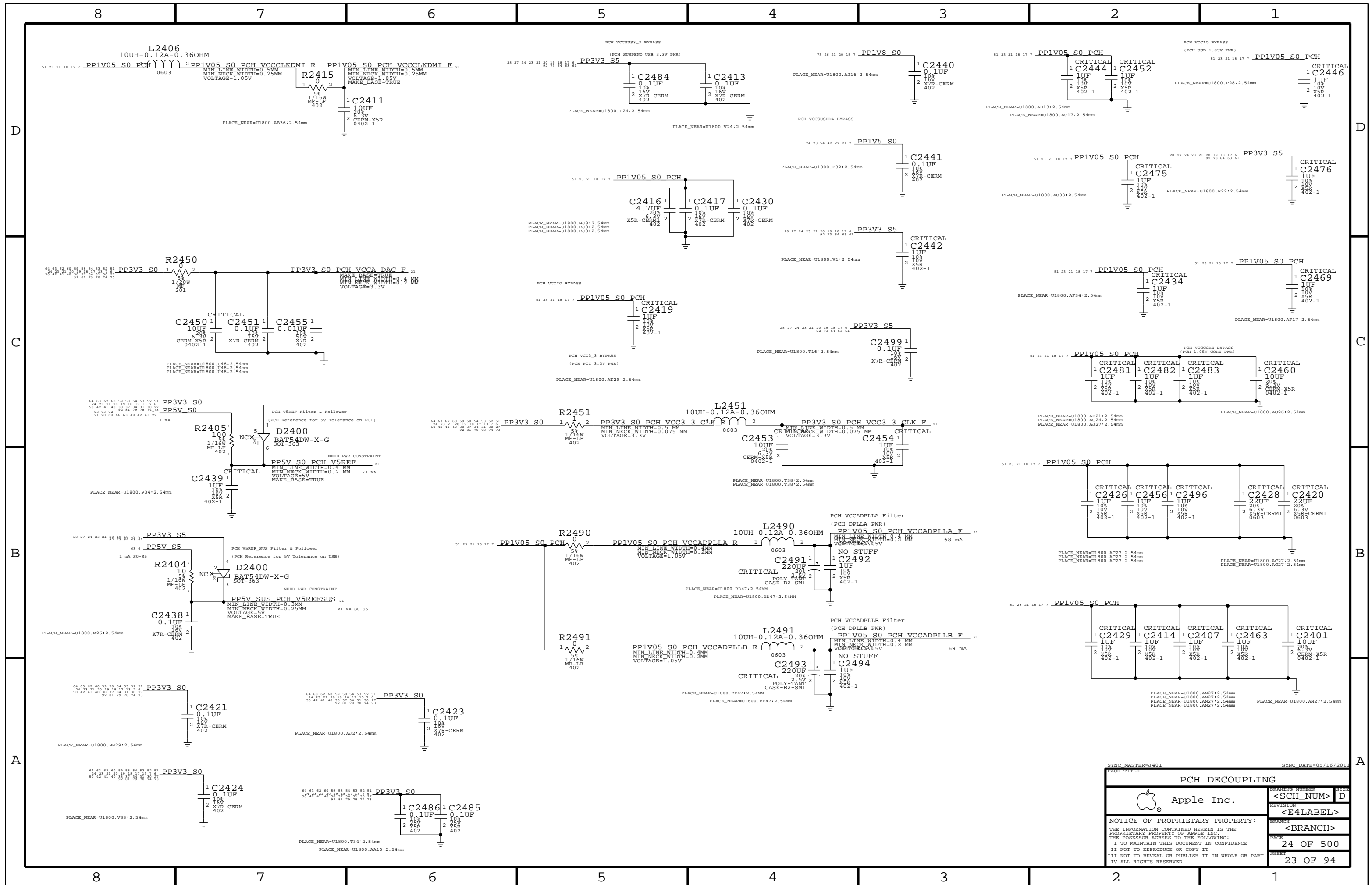


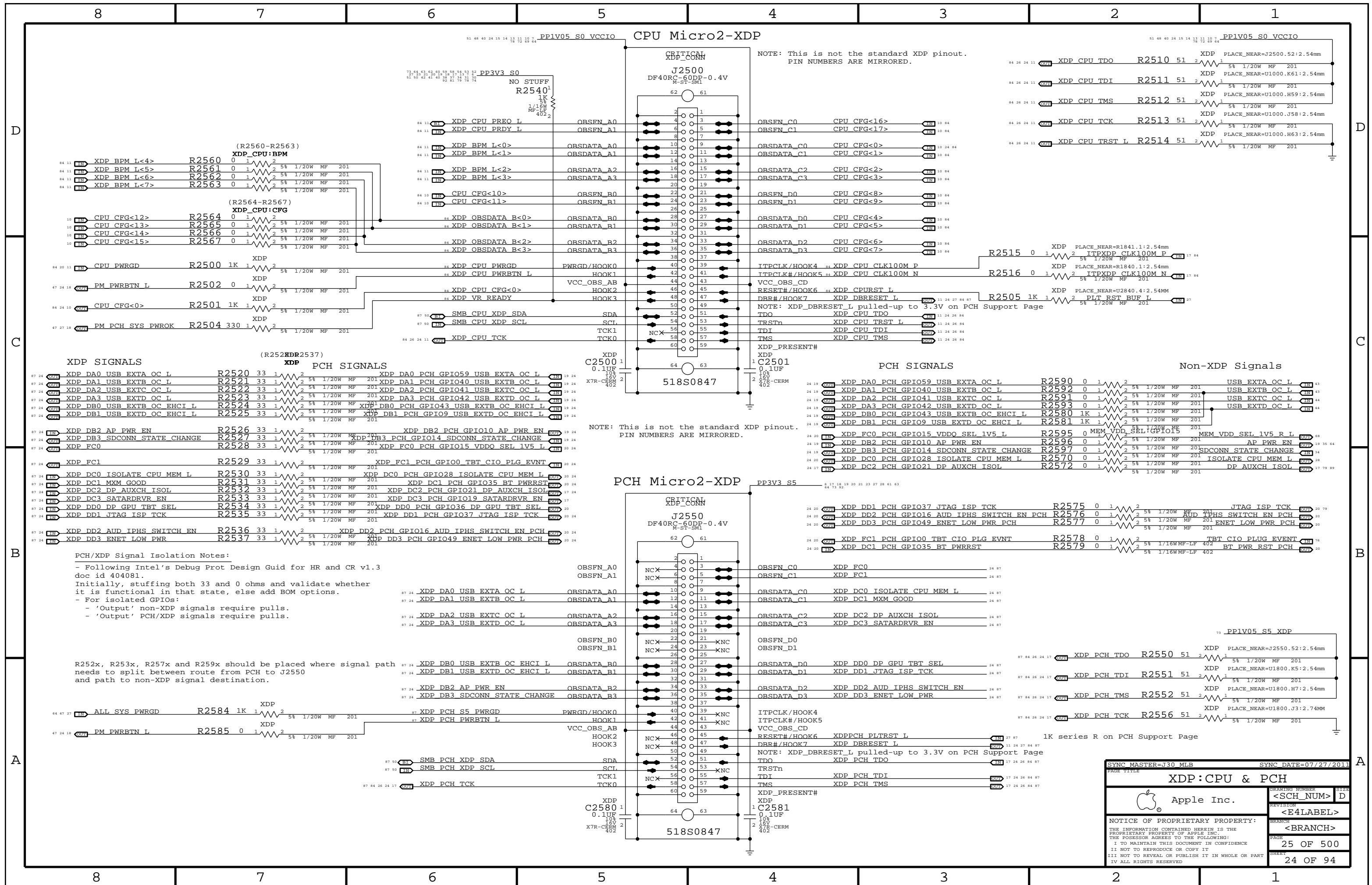


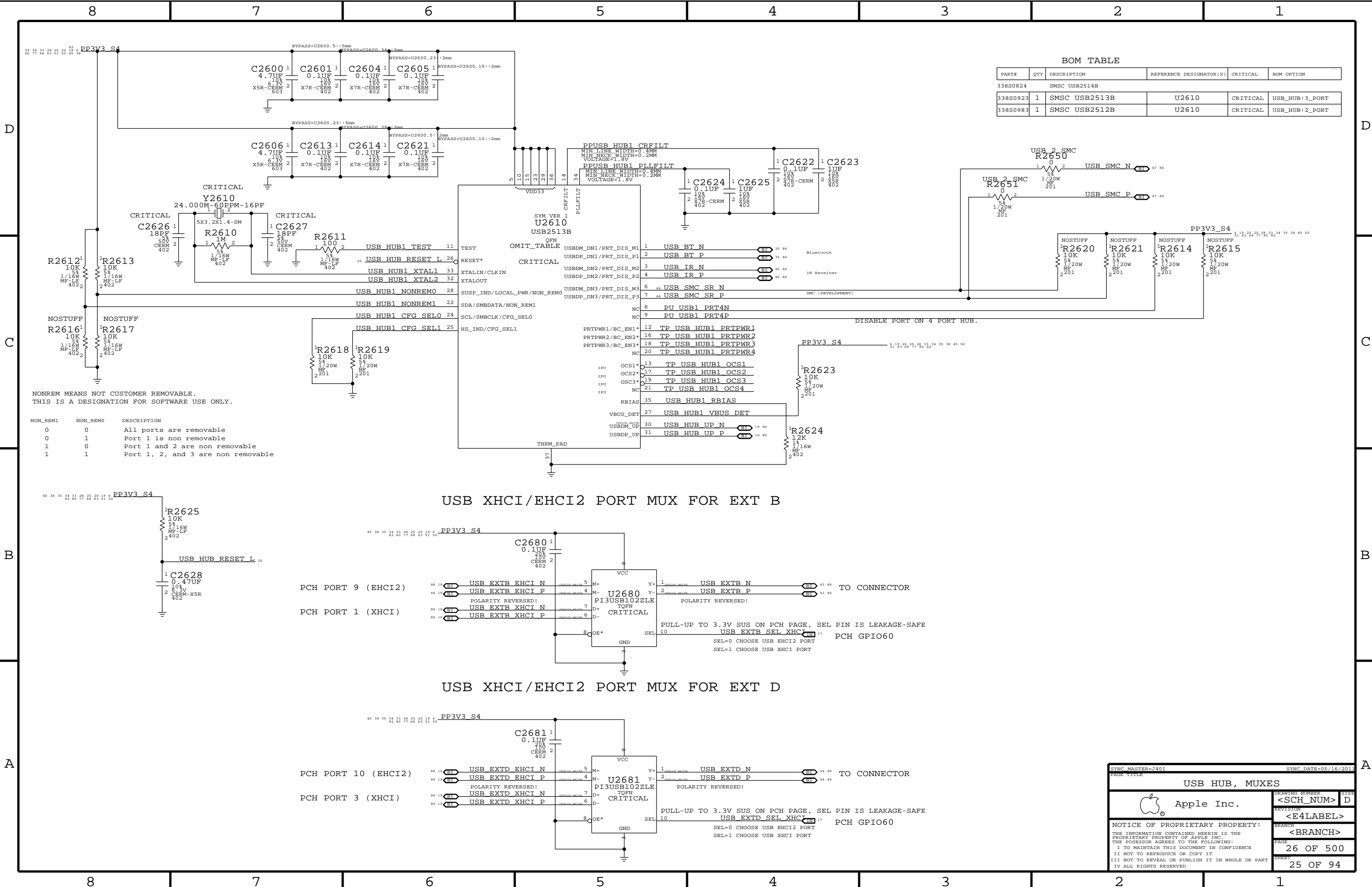








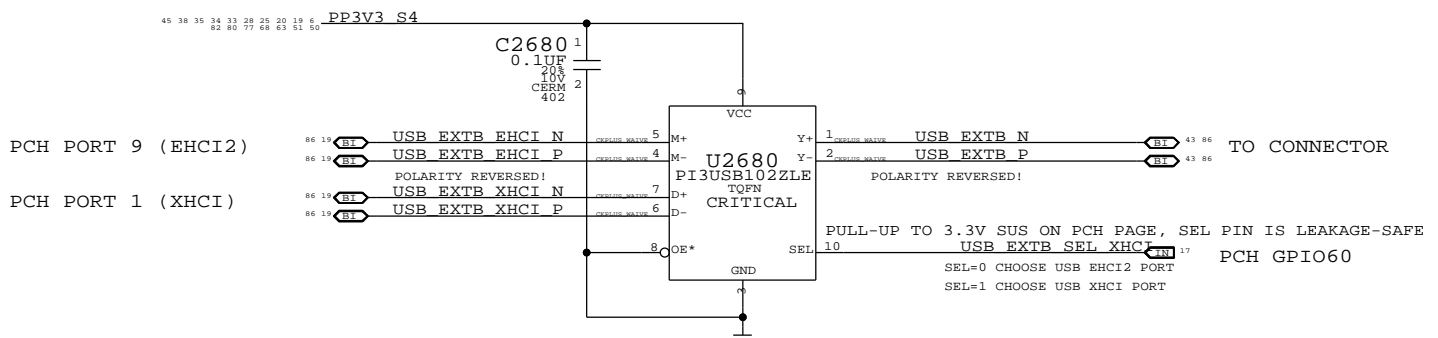




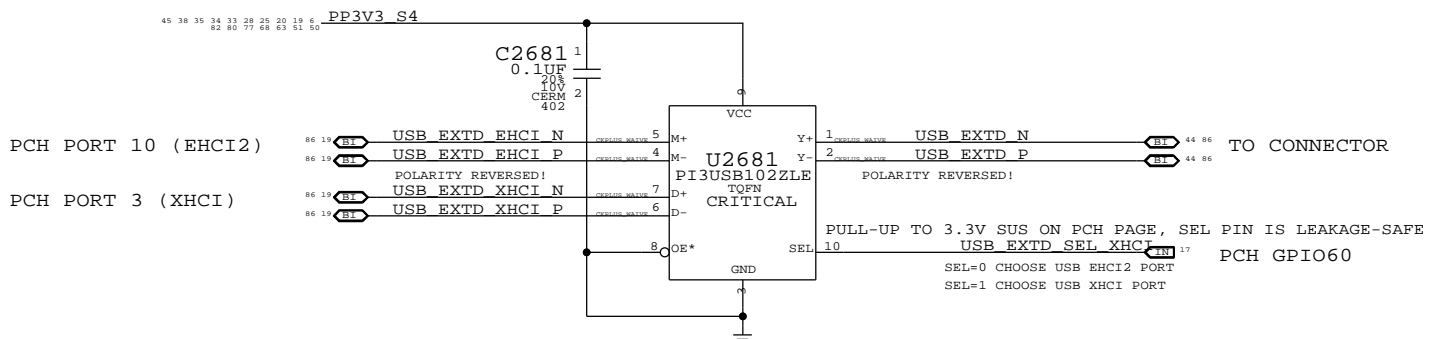
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL
338S0824		SMSC USB2514B		
338S0923	1	SMSC USB2513B	U2610	CRITICAL
338S0983	1	SMSC USB2512B	U2610	CRITICAL

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

USB XHCI/EHCI2 PORT MUX FOR EXT B



USB XHCI/EHCI2 PORT MUX FOR EXT D



SYNC MASTER=J401

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USB HUB, MUXES

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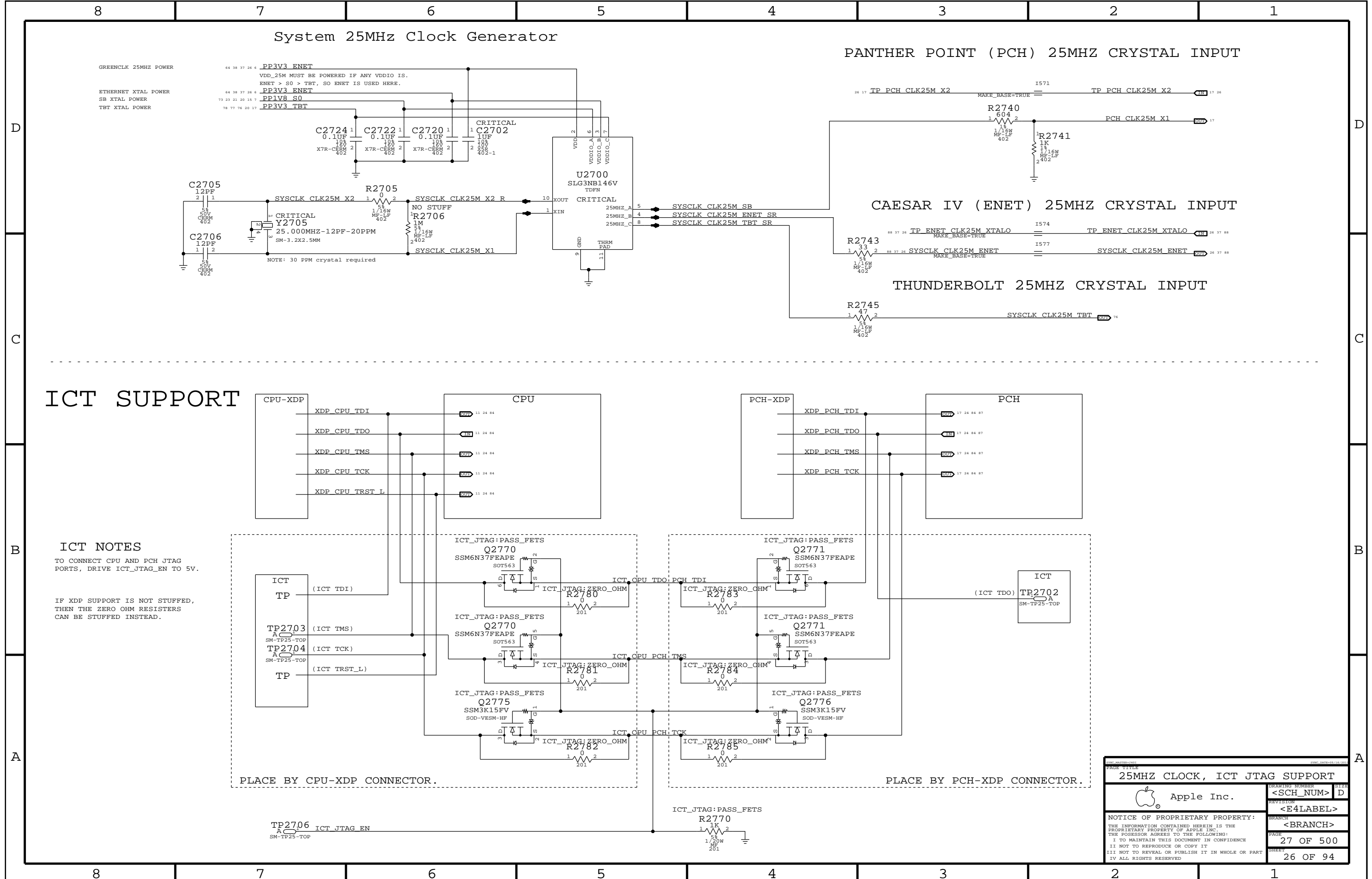
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ICT SUPPORT

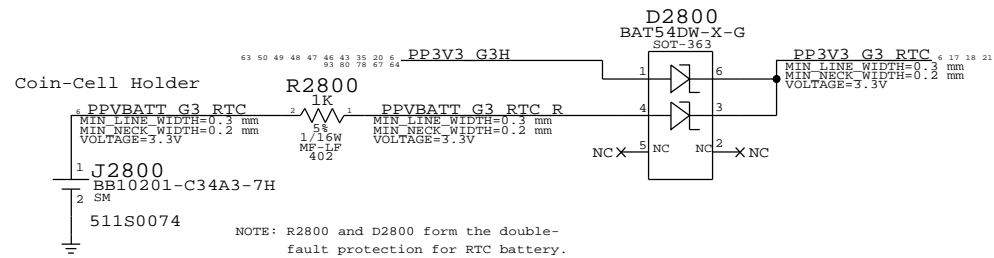
ICT NOTES

TO CONNECT CPU AND PCH JTAG PORTS, DRIVE ICT_JTAG_EN TO 5V.

IF XDP SUPPORT IS NOT STUFFED, THEN THE ZERO OHM RESISTORS CAN BE STUFFED INSTEAD.

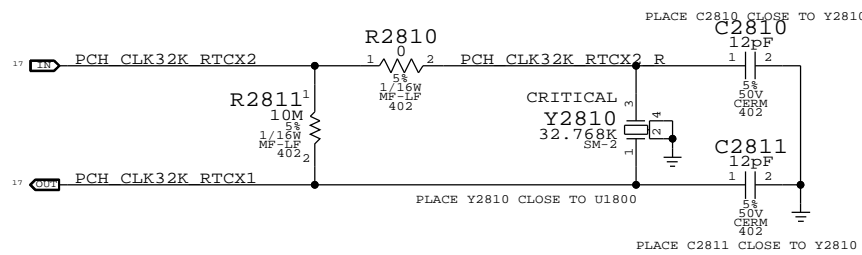
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25MHZ CLOCK, ICT JTAG SUPPORT		<SCH_NUM>		D
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RTC Power Sources



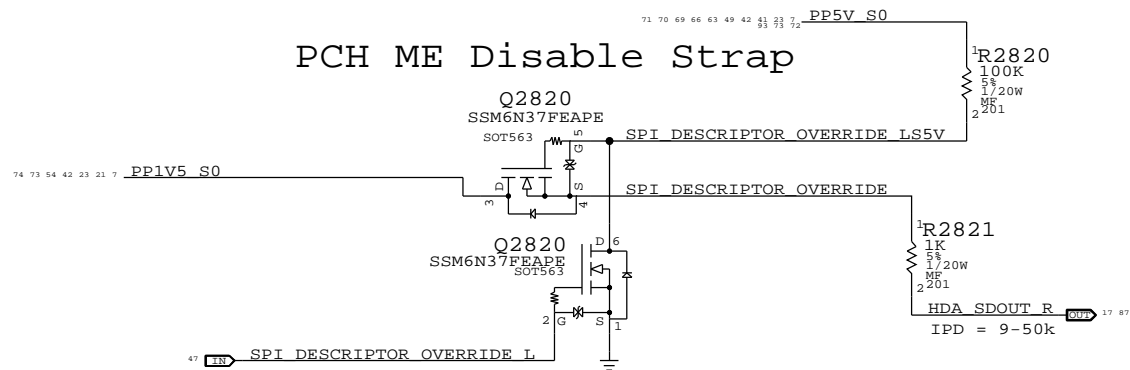
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PCH RTC Crystal

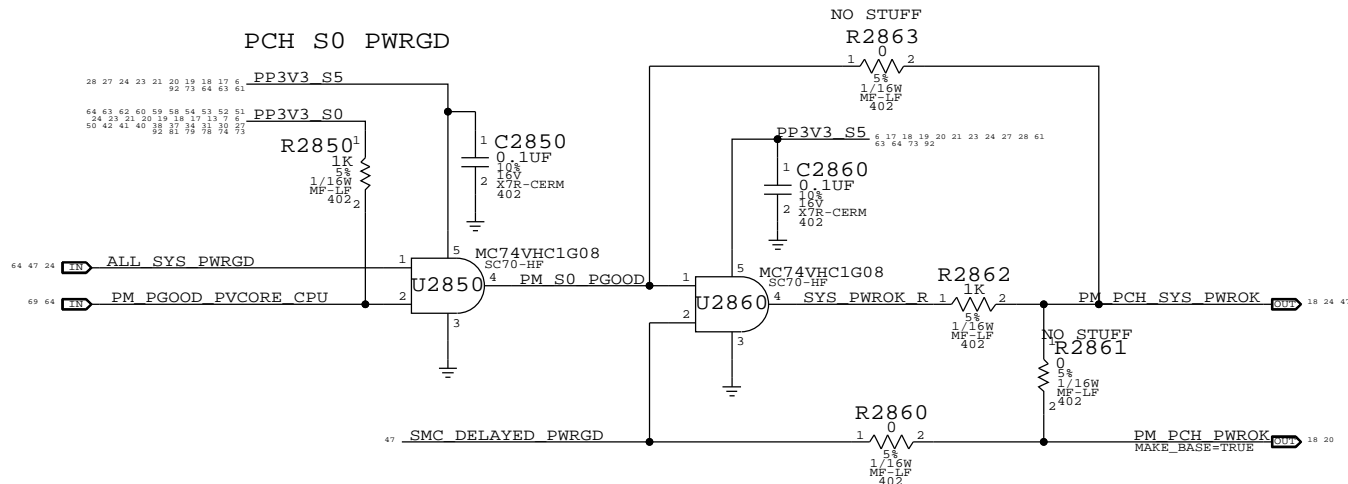


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

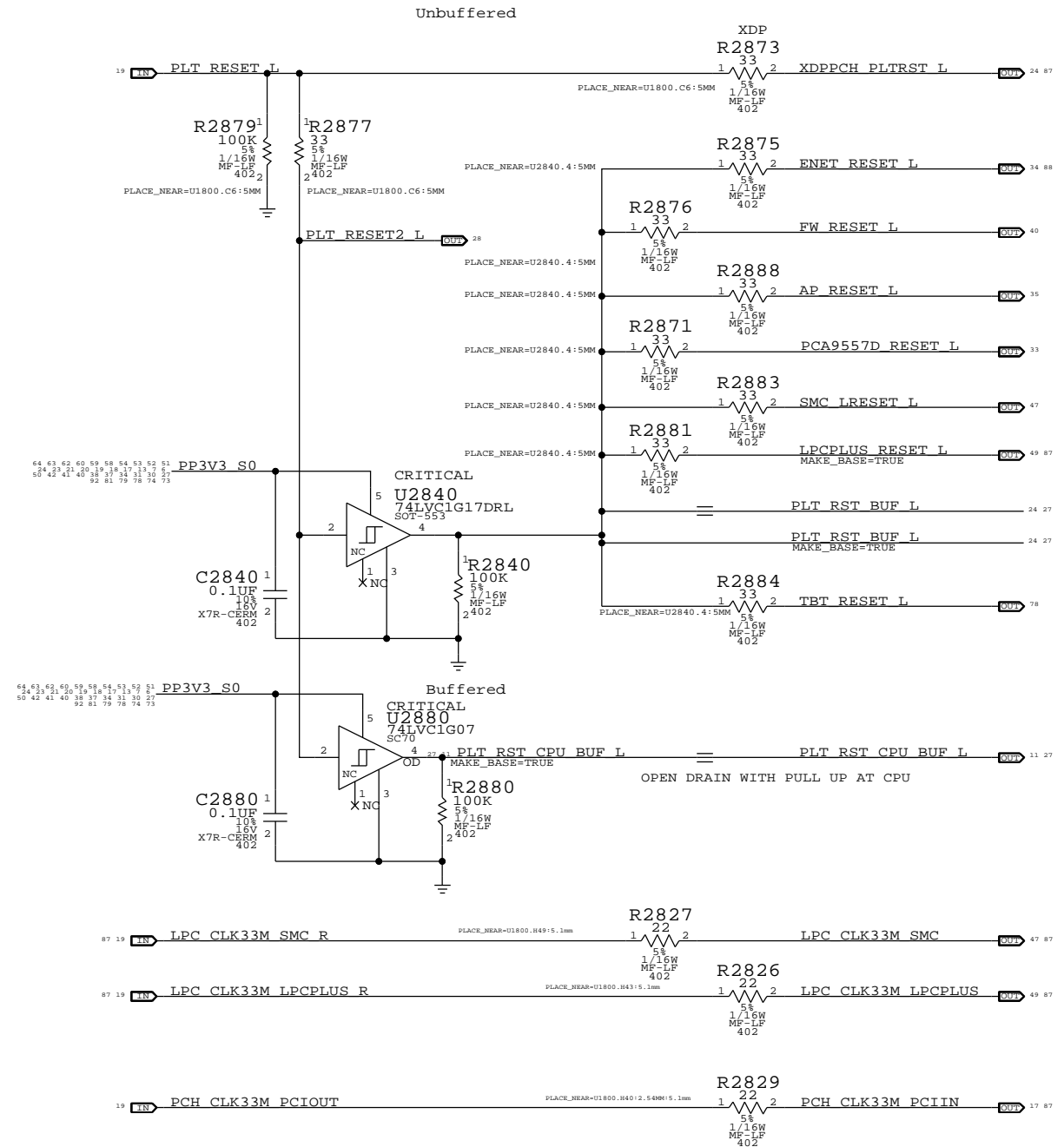
PCH ME Disable Strap



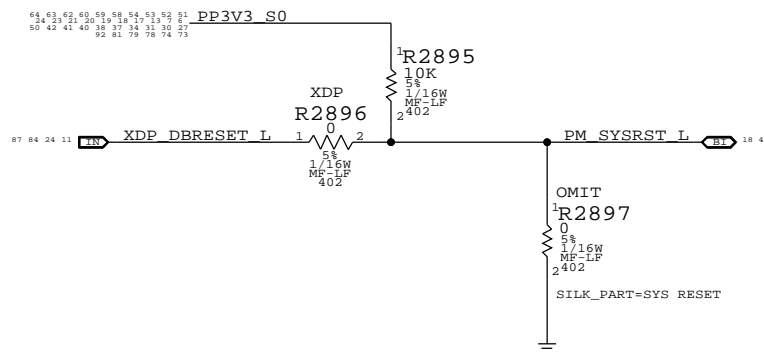
PCH S0 PWRGD



Platform Reset Connections



PCH Reset Button



SYMC PART# 74201		SYMC DATE=05/16/2011	
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RTC SUPPORT, RESETS		DRAWING NUMBER	
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the S0-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

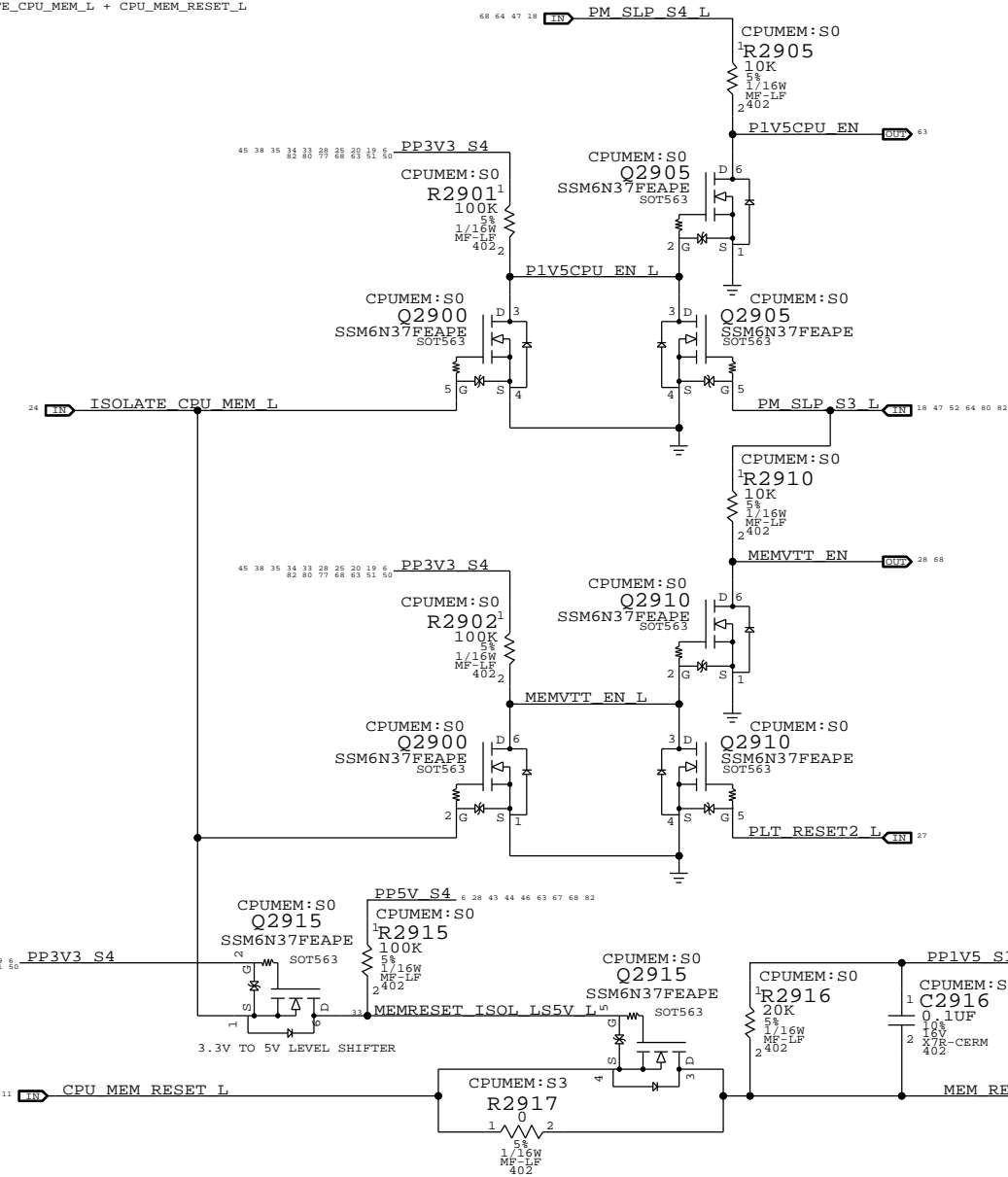
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

Plv5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

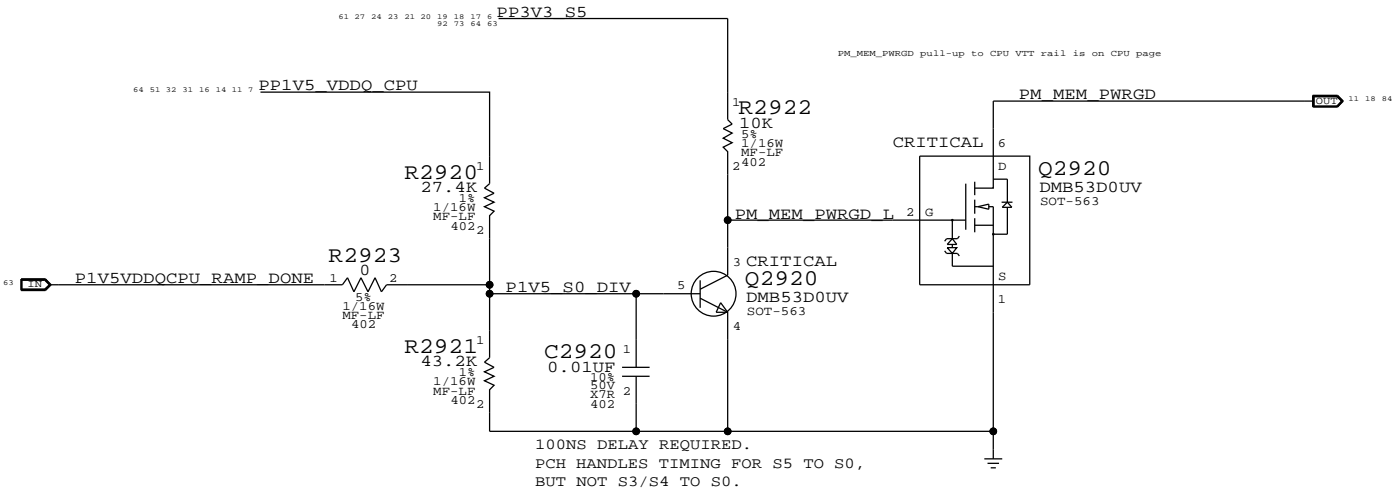
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



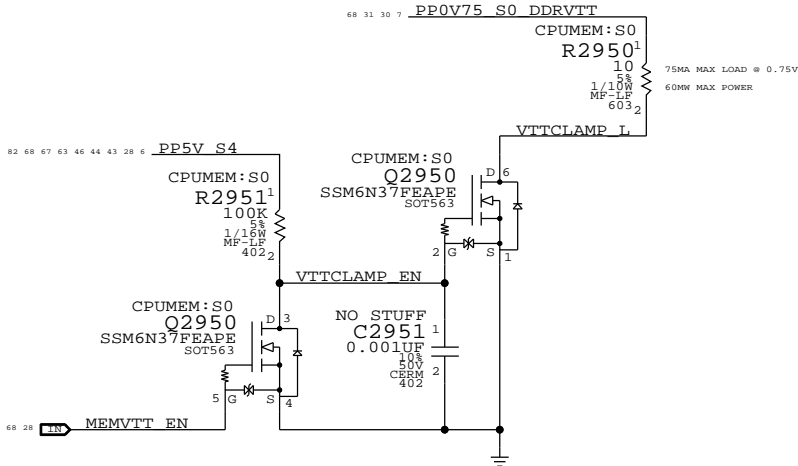
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1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3

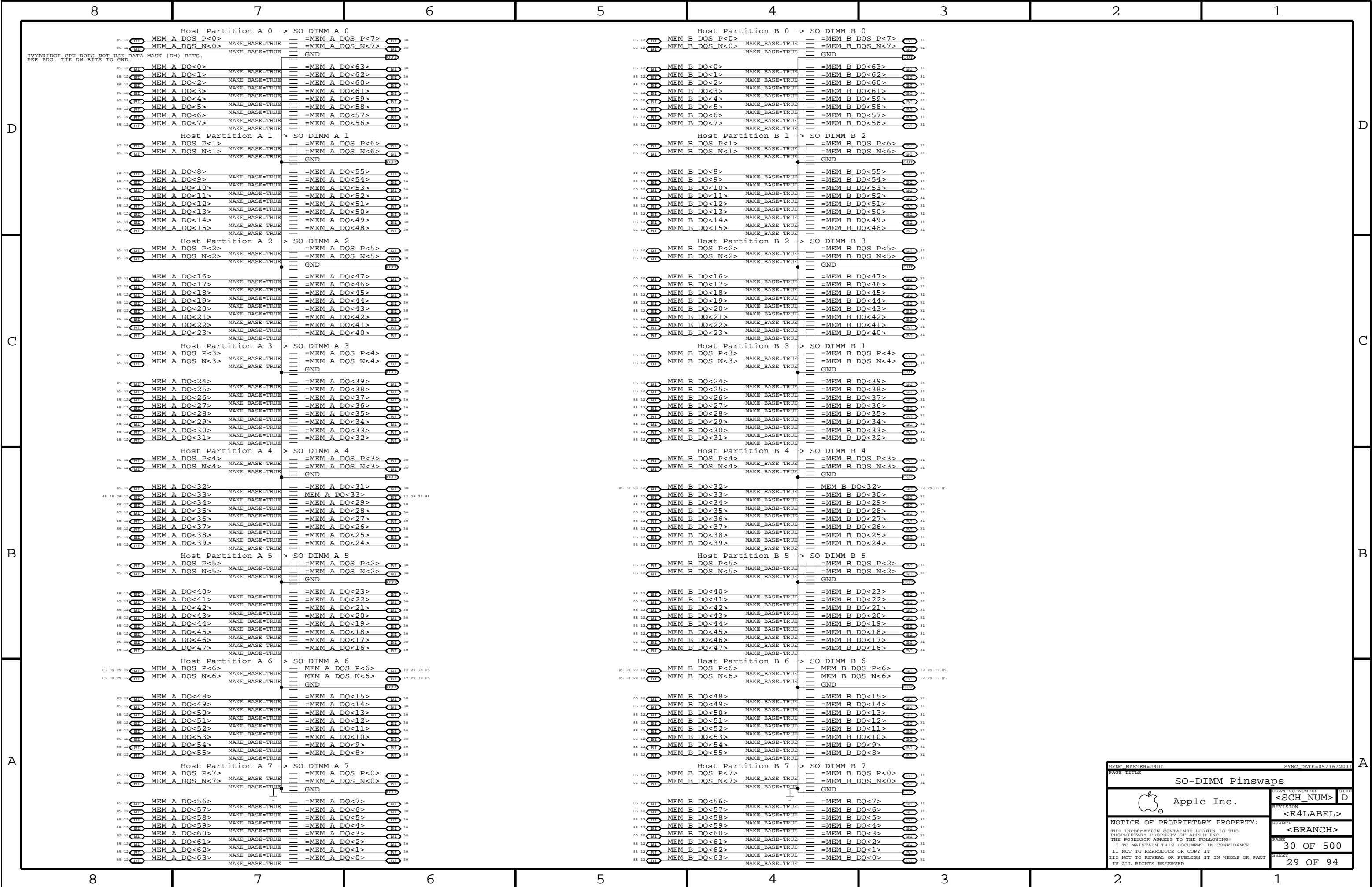


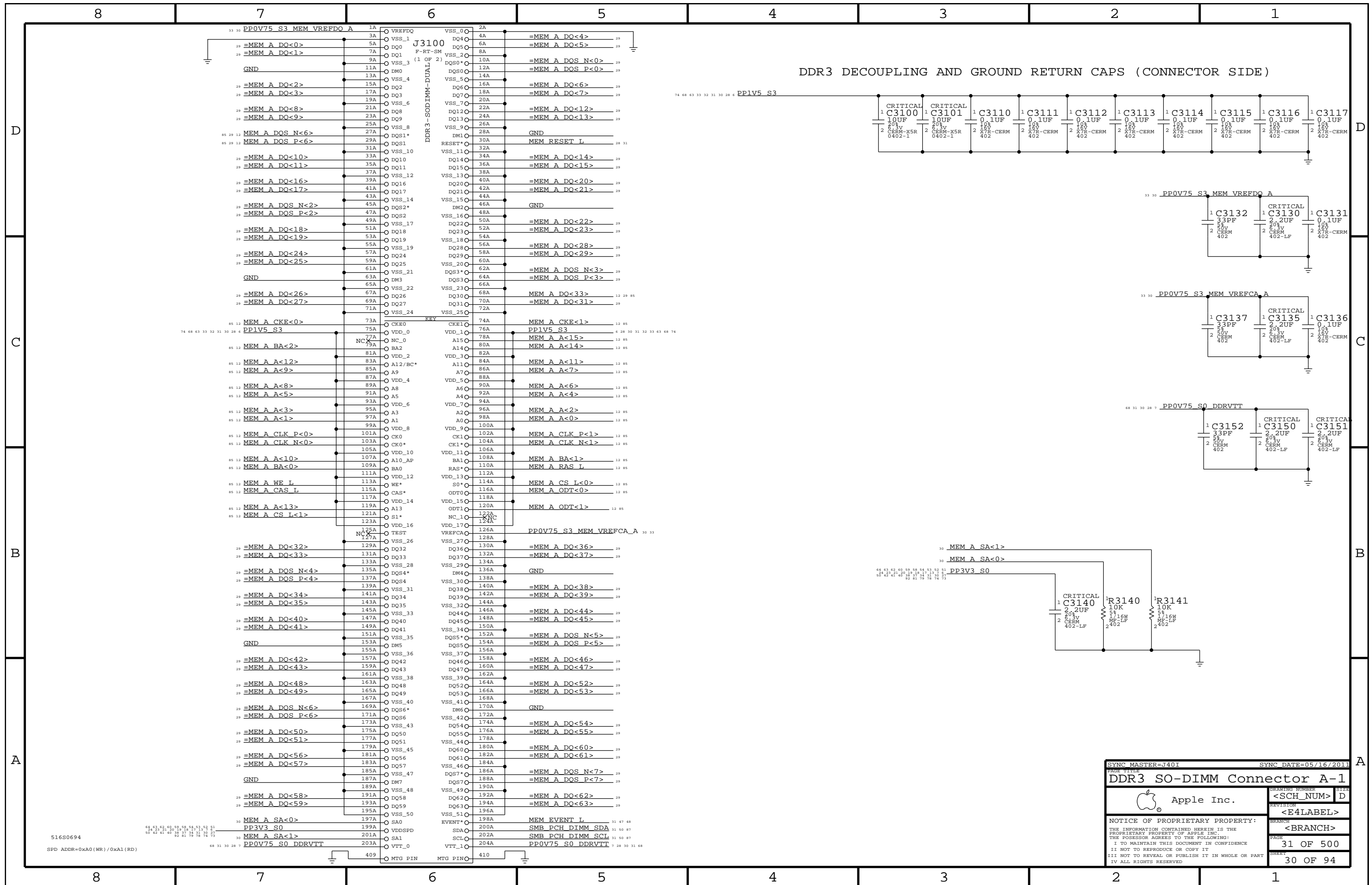
Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPUMEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPUMEM_RESET_L	1	1
1	0	1	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	1	1	X	1	0	0
S3	4	0	0	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPUMEM_RESET_L	1	1

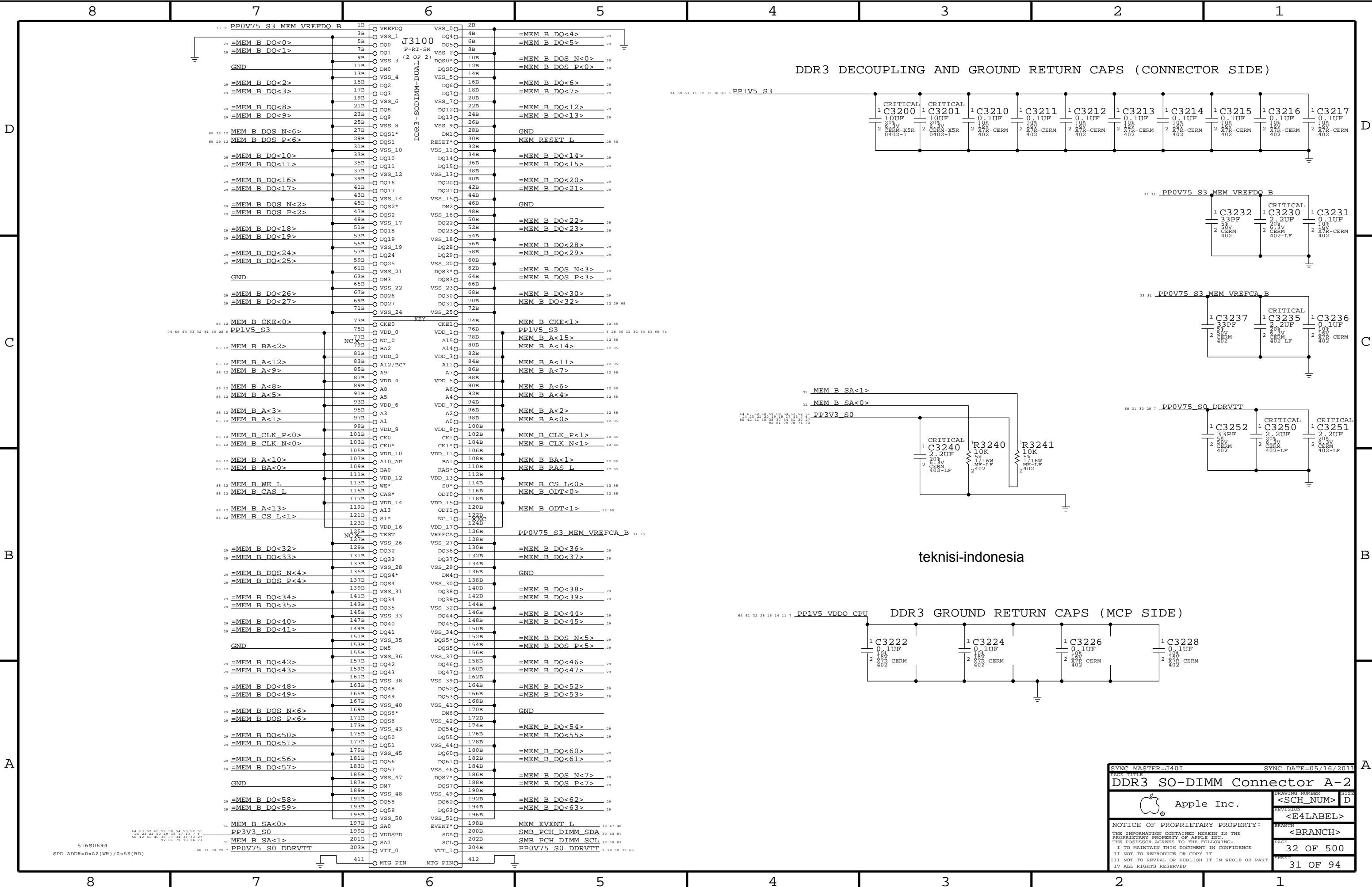
(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.


NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

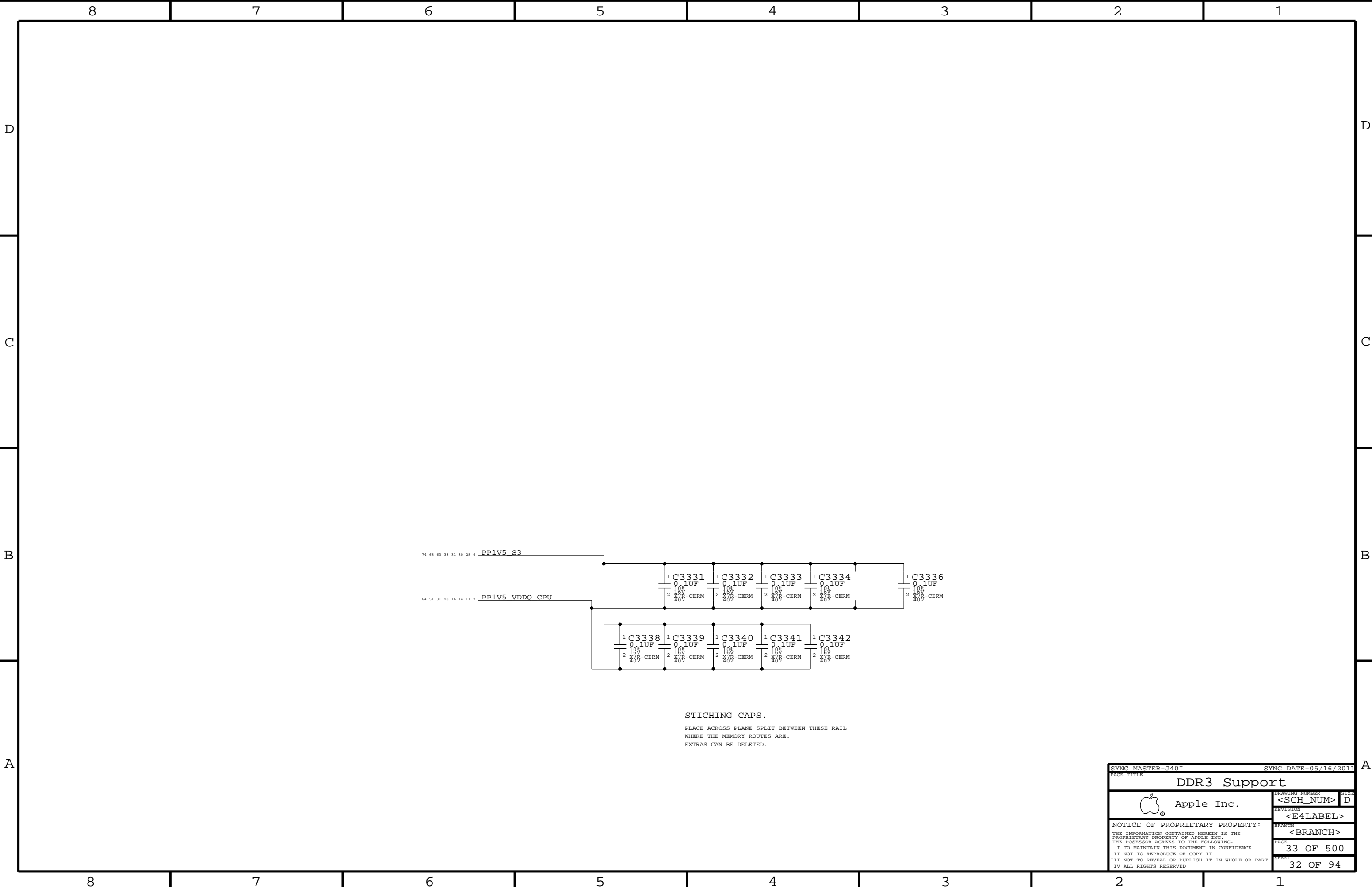
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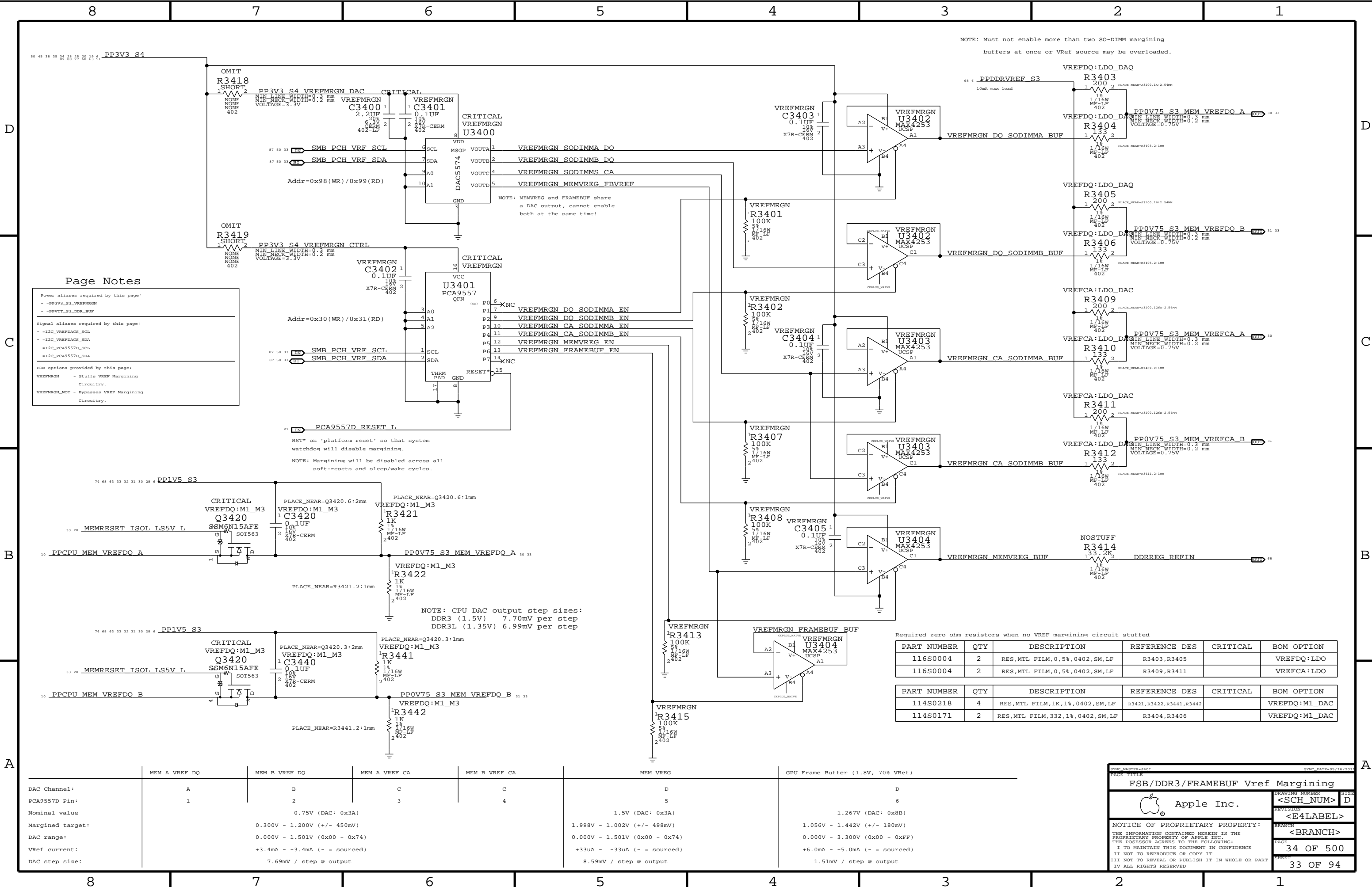






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		PAGE	
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		SHEET	
		31 OF 94	





Page Notes

Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DCR_BUF

Signal aliases required by this page:

- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

- VREFMRGN - Stuffs VREF Margining Circuitry.
- VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYMC PART#=3401SYMC DATE=05/16/2011

FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

<SCH_NUM> D

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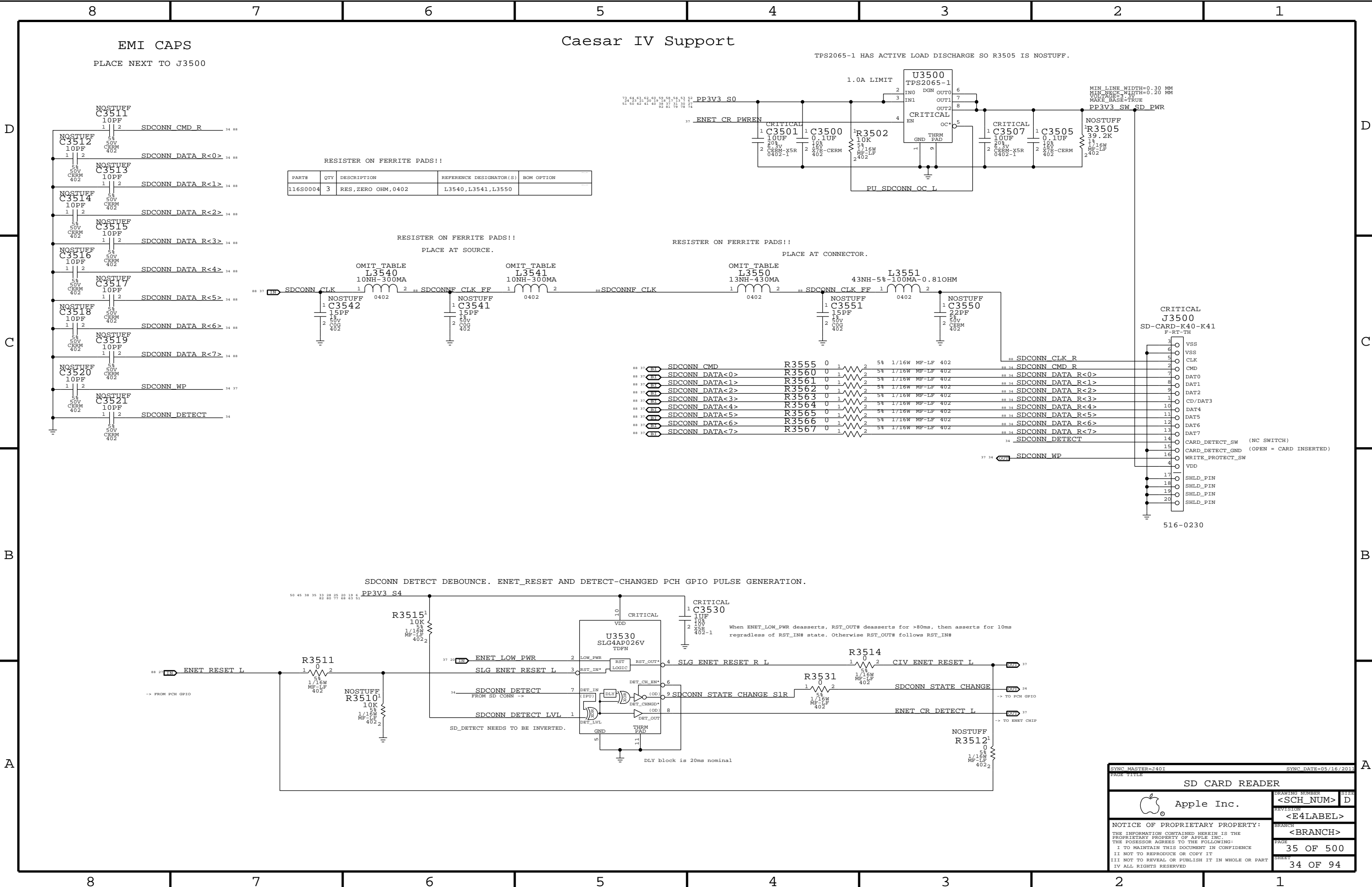
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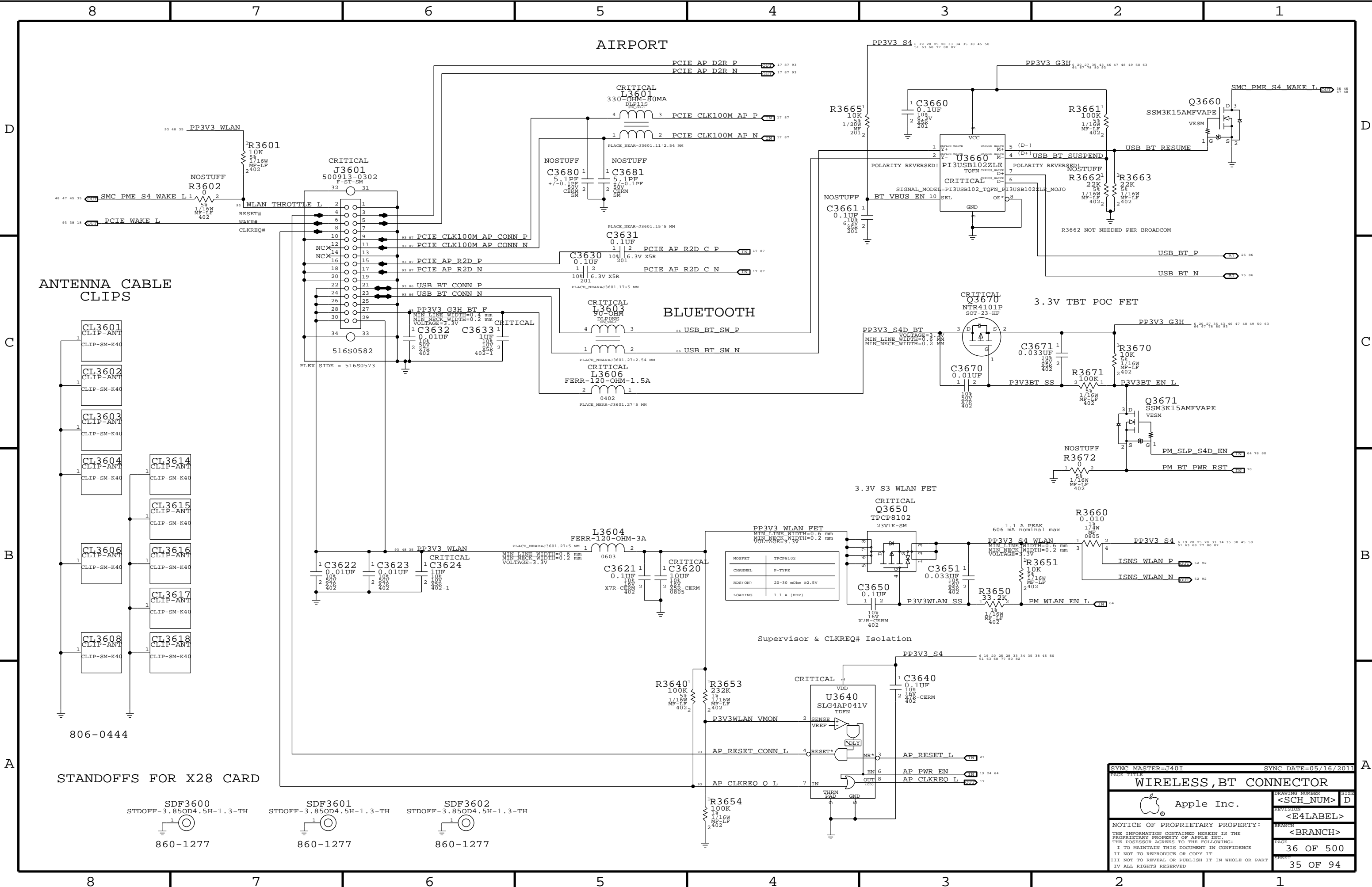
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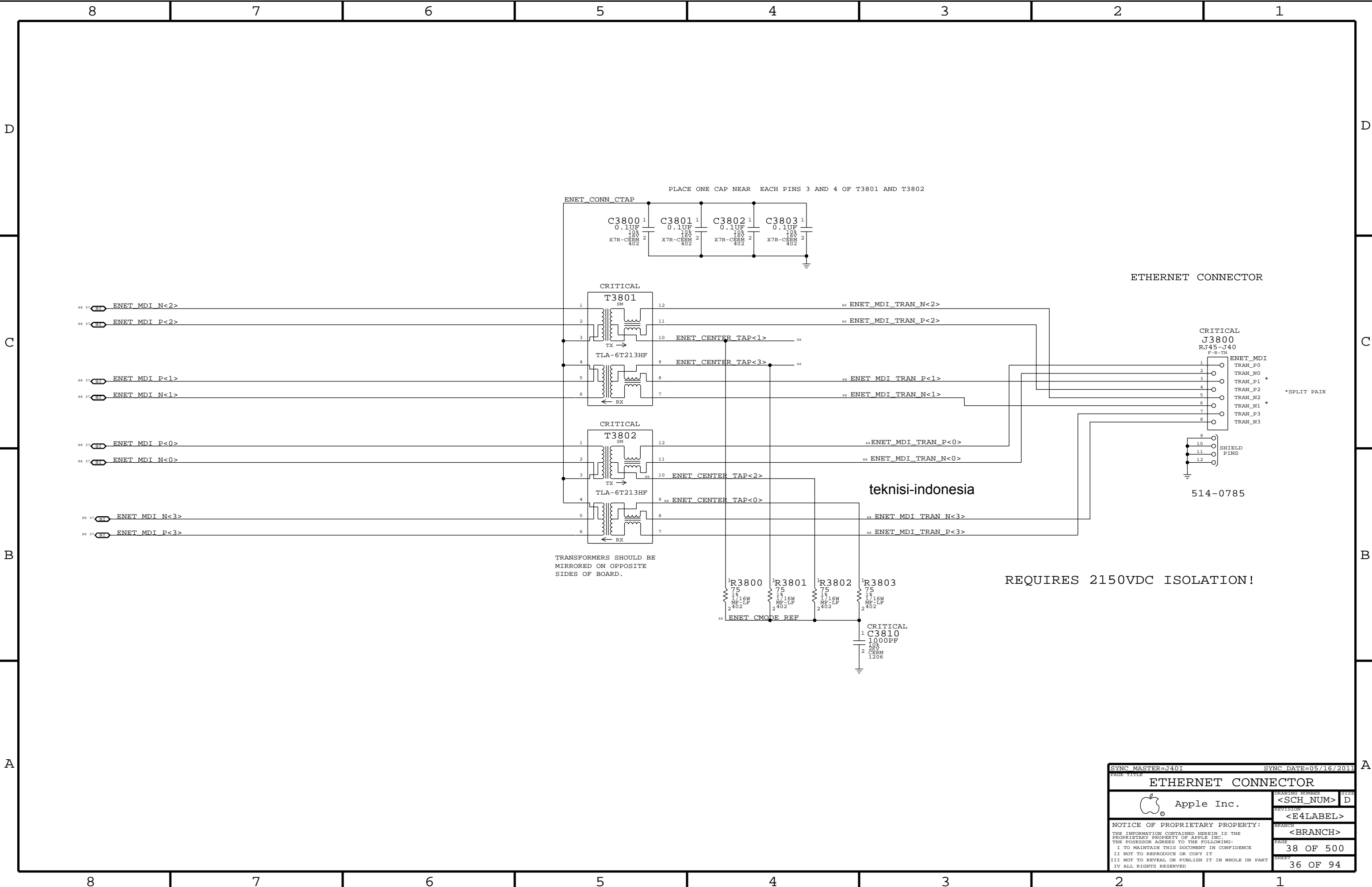
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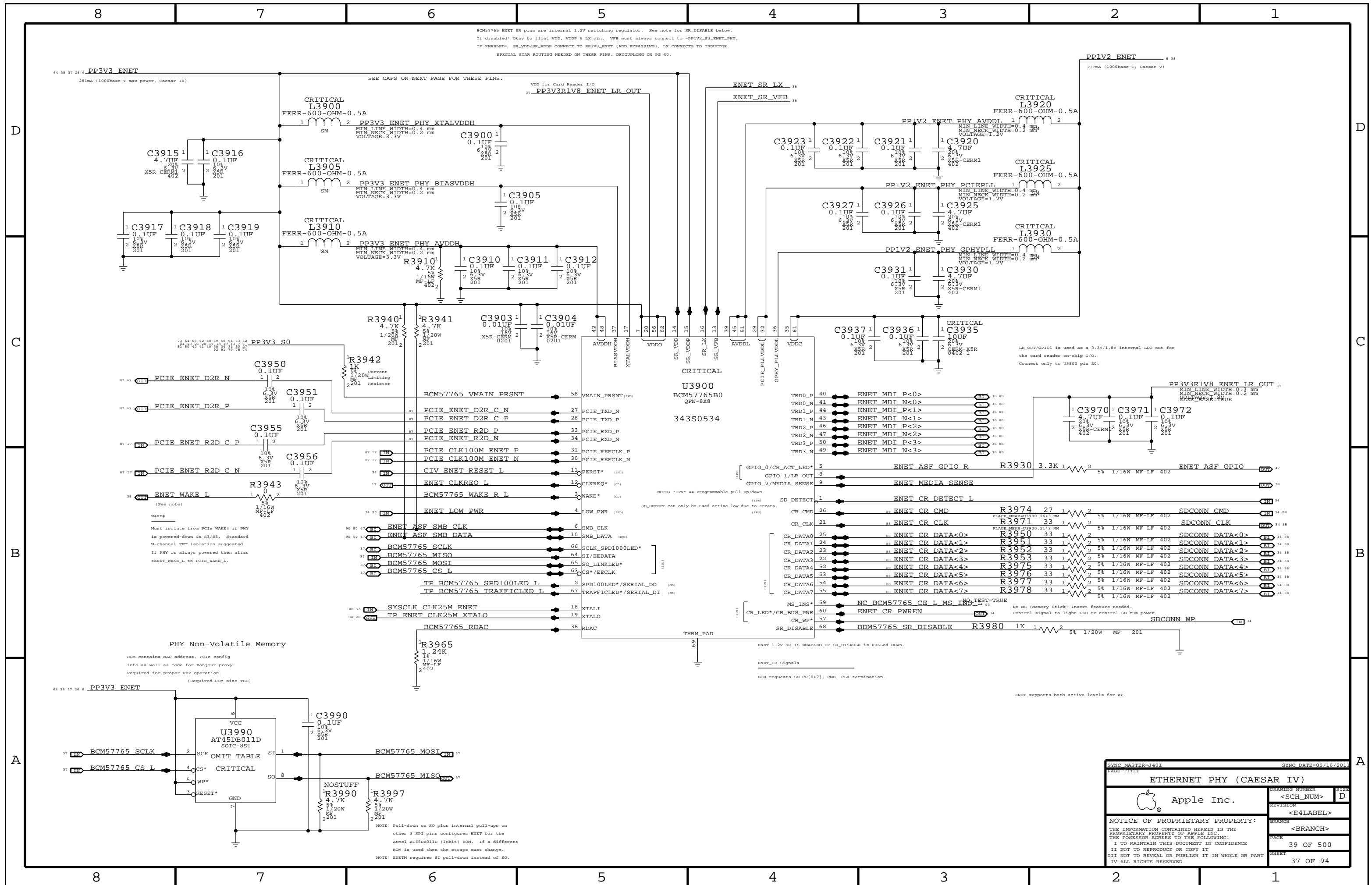
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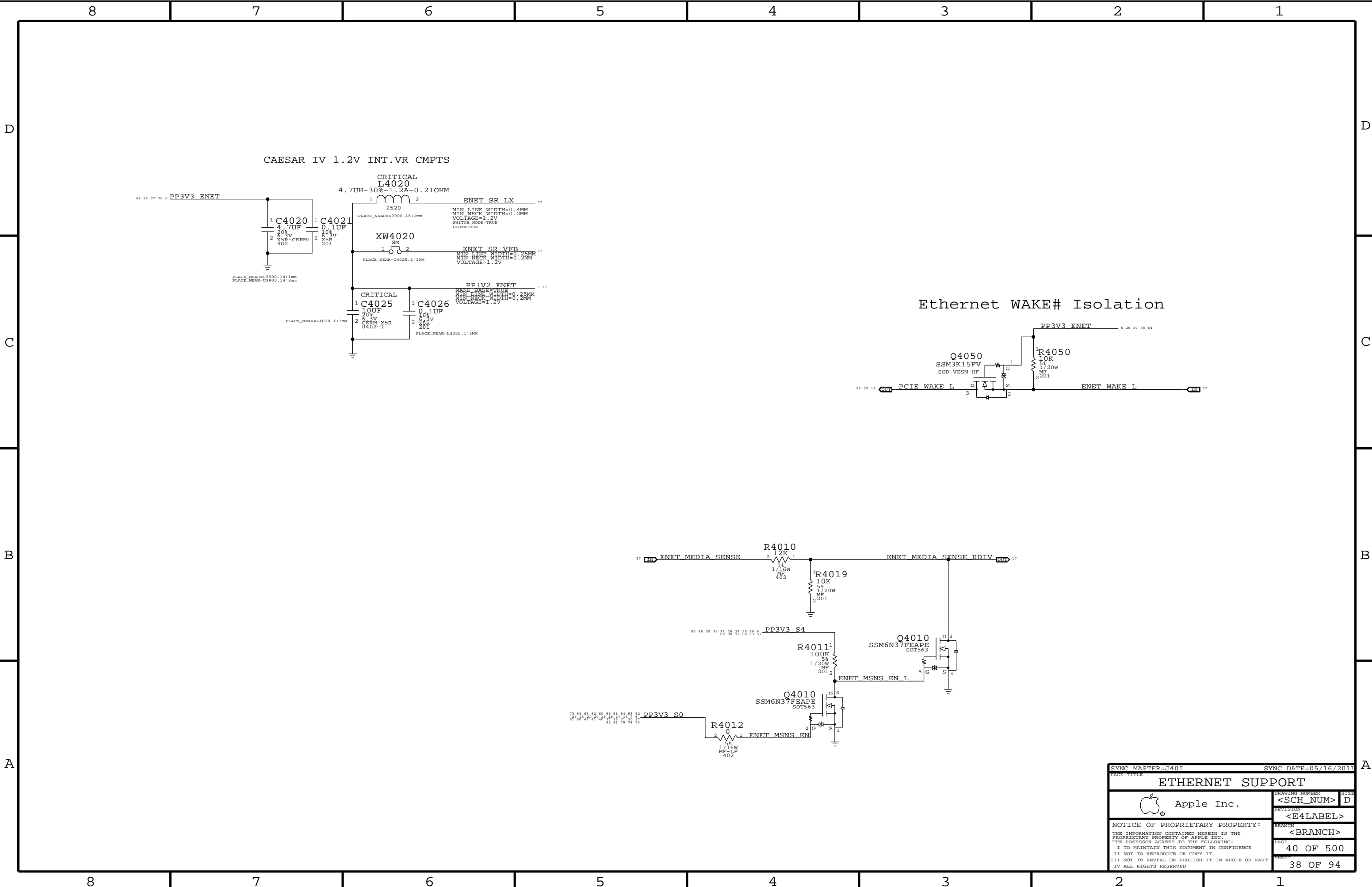





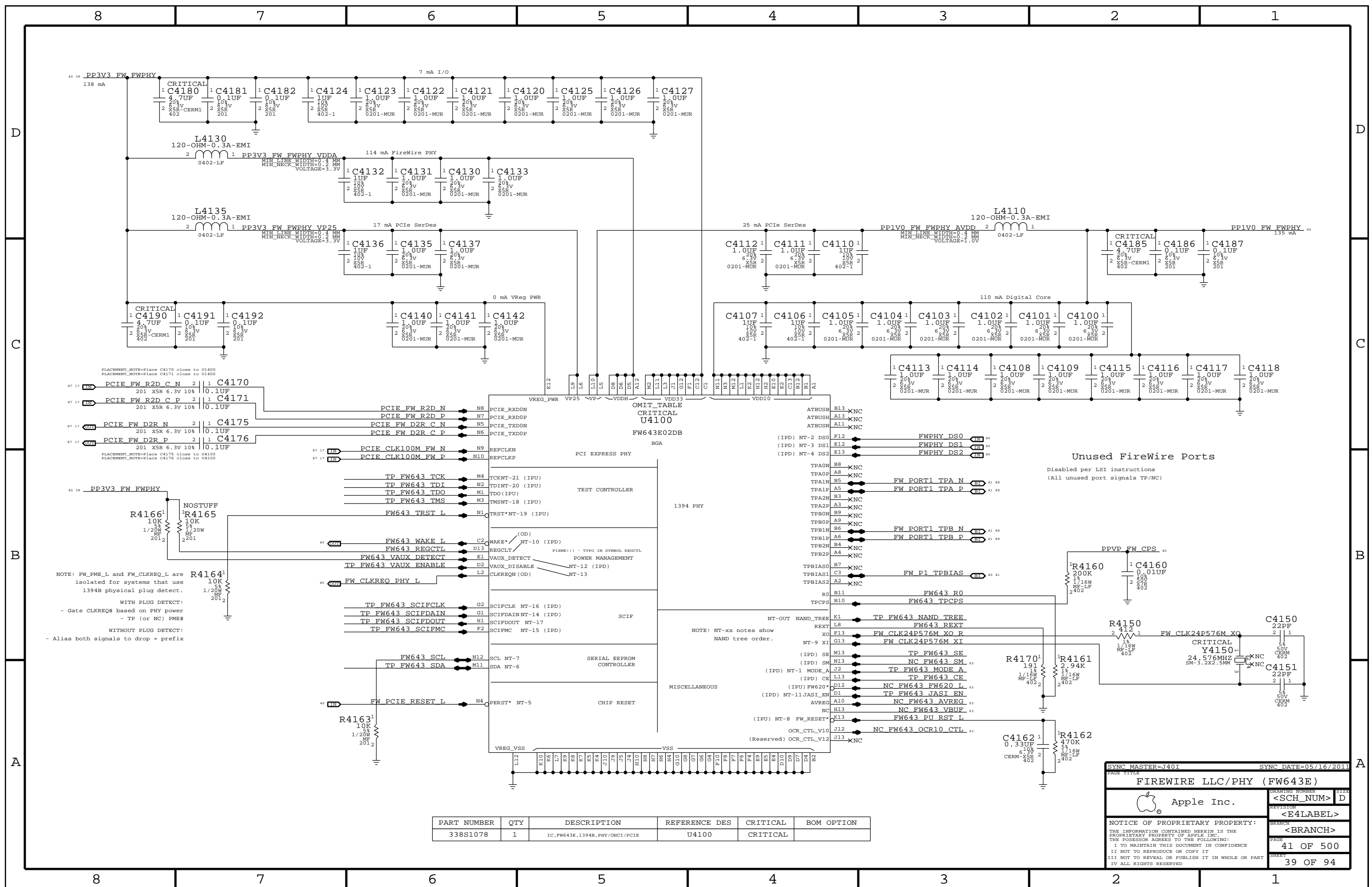
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		35 OF 94	

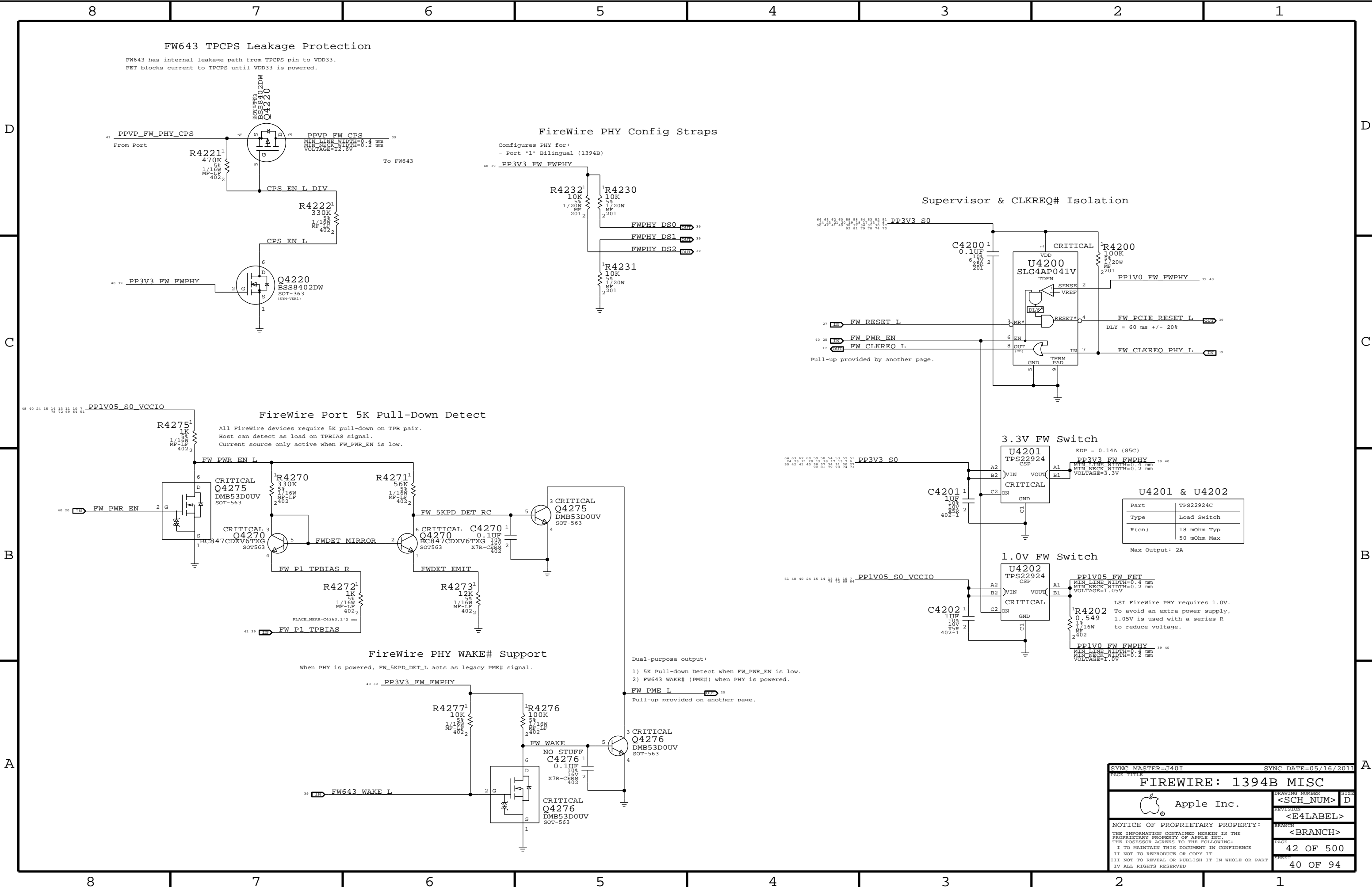






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FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.

FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

Supervisor & CLKREQ# Isolation

FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

Dual-purpose output:

- 1) 5K Pull-down Detect when FW_PWR_EN is low.
- 2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

3.3V FW Switch

EDP = 0.14A (85C)

1.0V FW Switch


U4201 & U4202

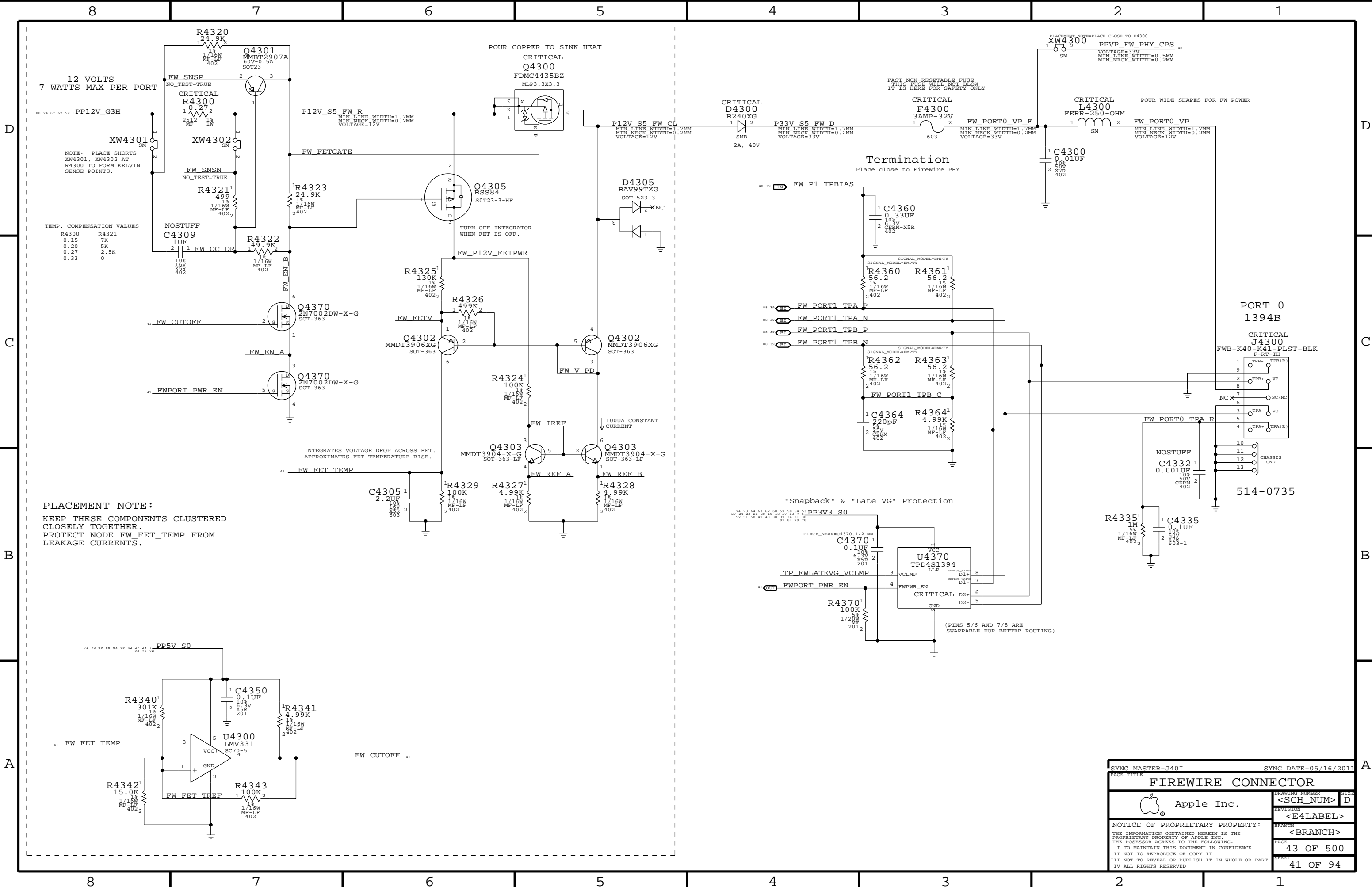
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ
	50 mOhm Max

Max Output: 2A

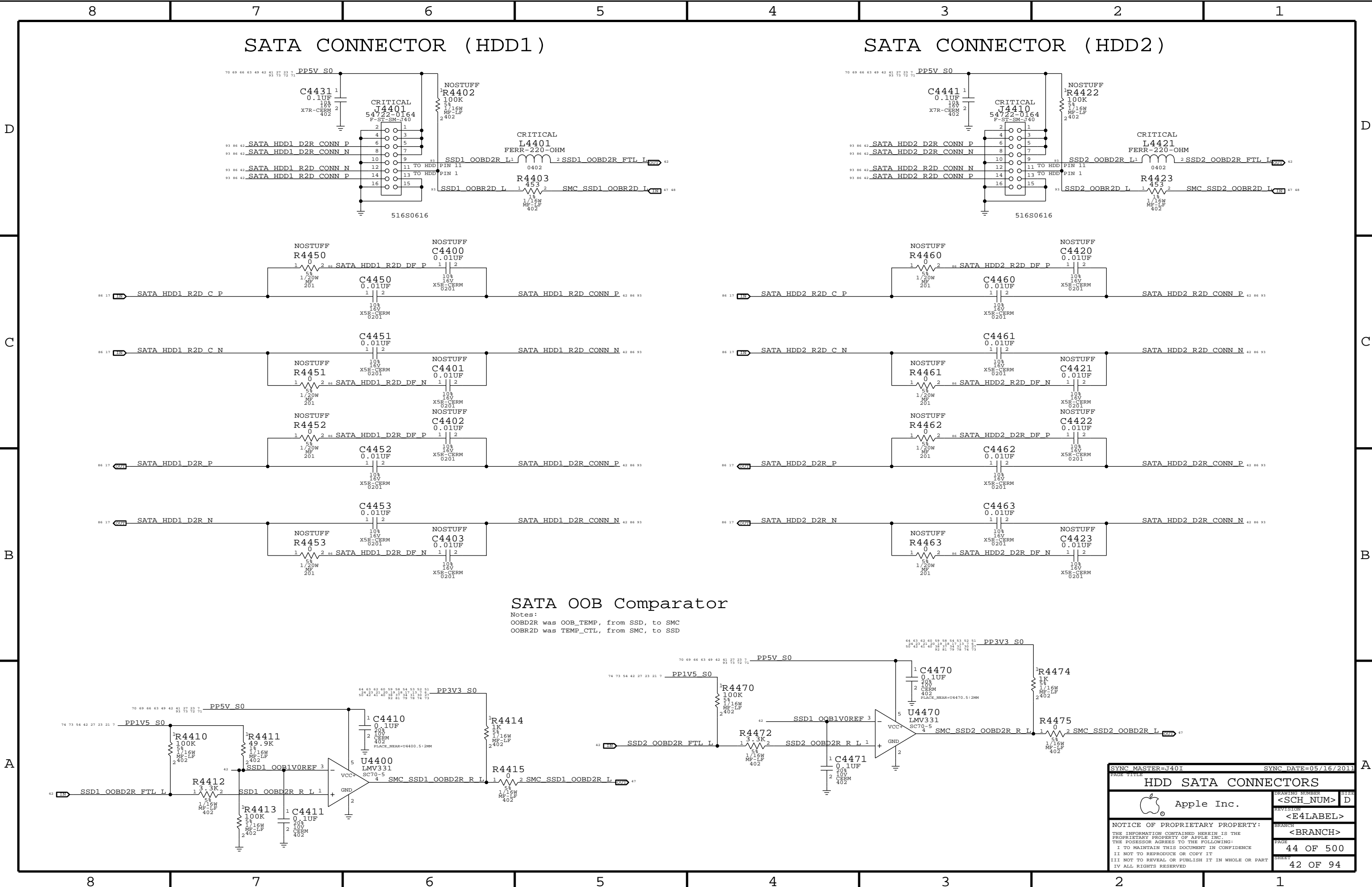
LSI FireWire PHY requires 1.0V.


To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

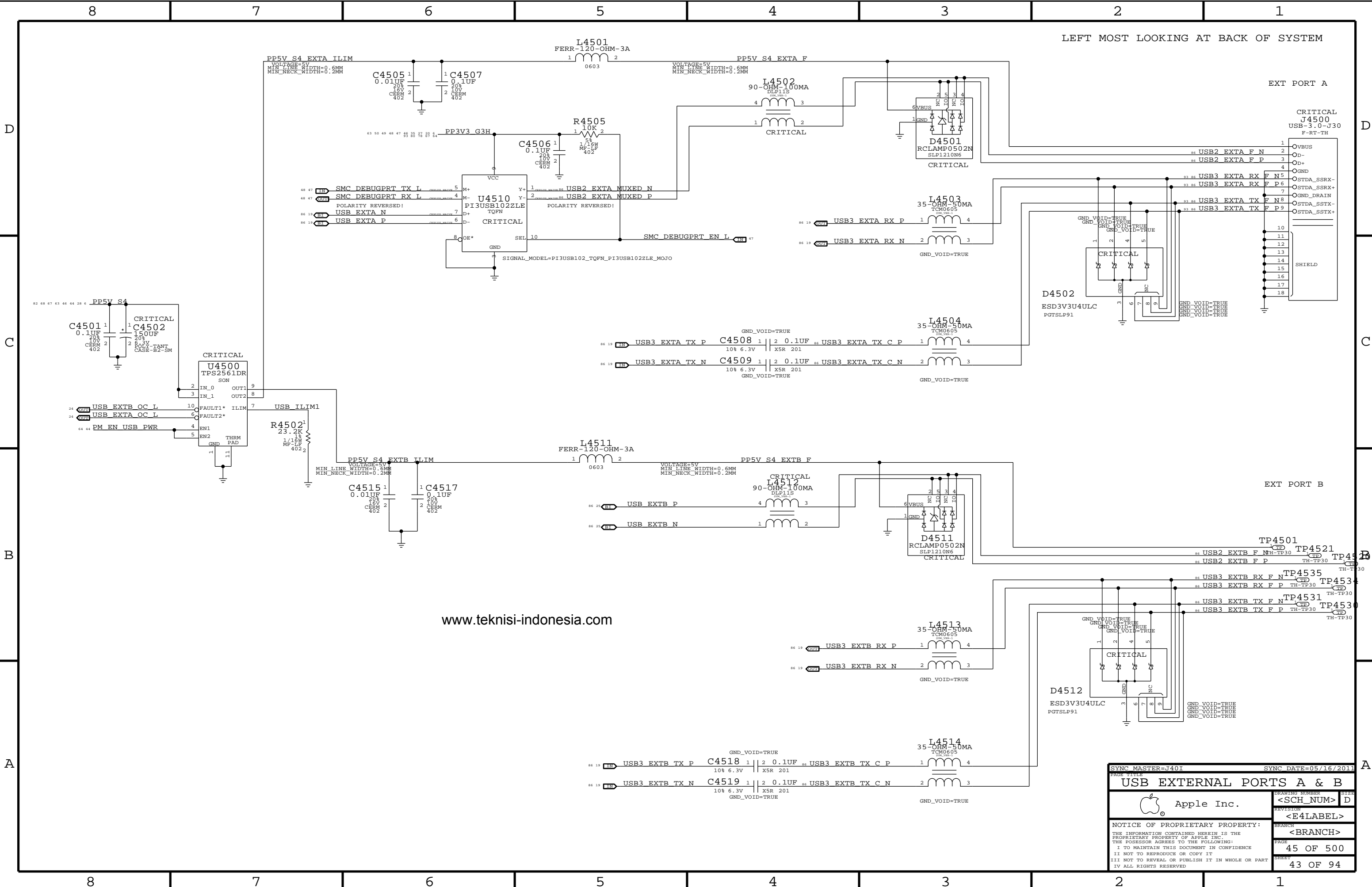
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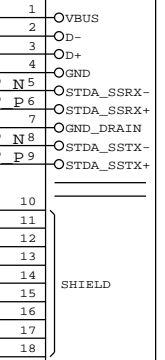
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		<BRANCH>	
		PAGE	44 OF 500
		SHEET	42 OF 94



LEFT MOST LOOKING AT BACK OF SYSTEM

EXT PORT A

CRITICAL
J4500
USB-3.0-J30
F-RT-TH




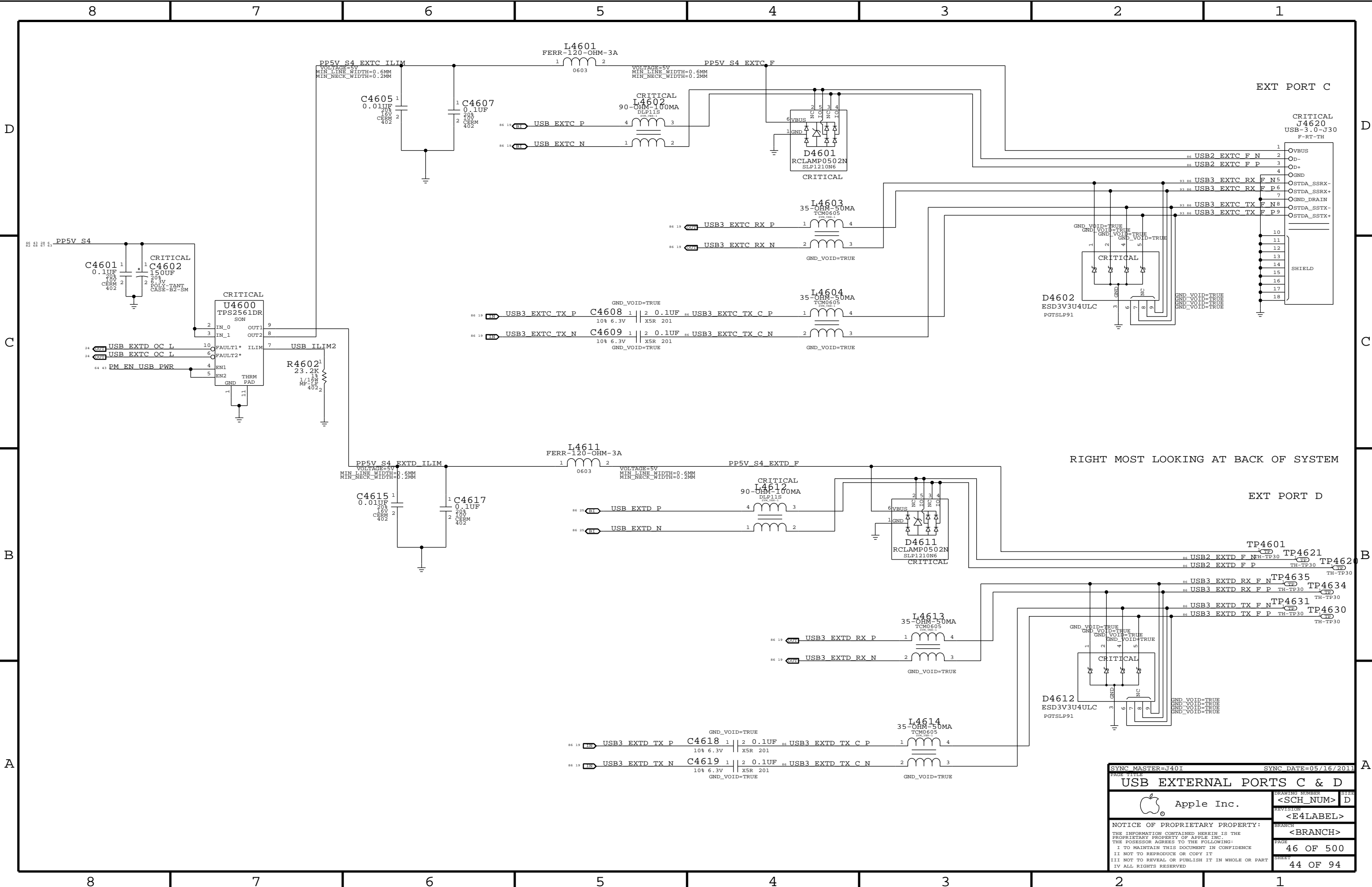
D4502
ESD3V3U4ULC
PGTSLP91


EXT PORT B

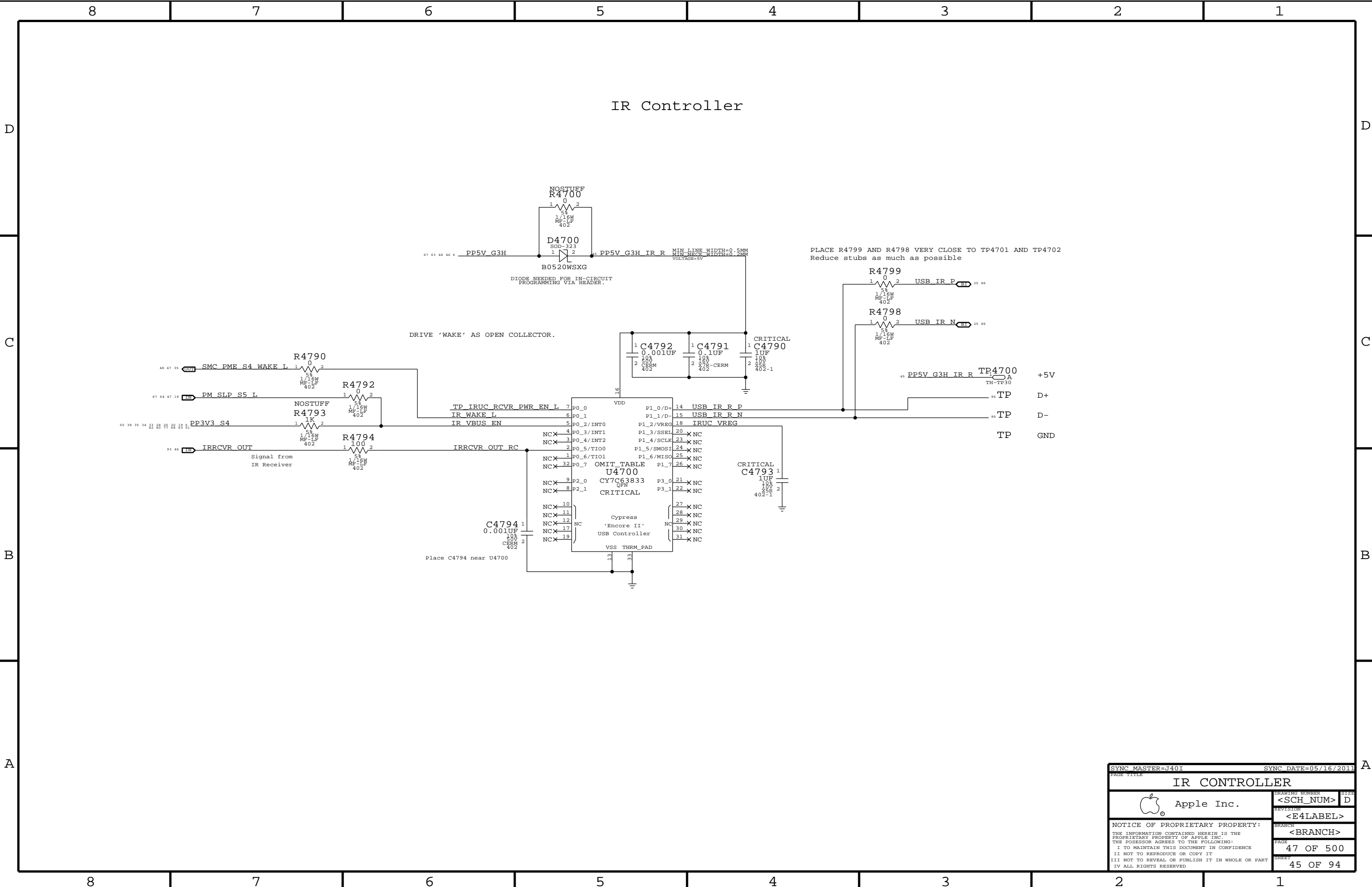
TP4501
TP4521
TP4535
TP4531
TP4530

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USB EXTERNAL PORTS C & D		<SCH_NUM>	
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		44 OF 94	



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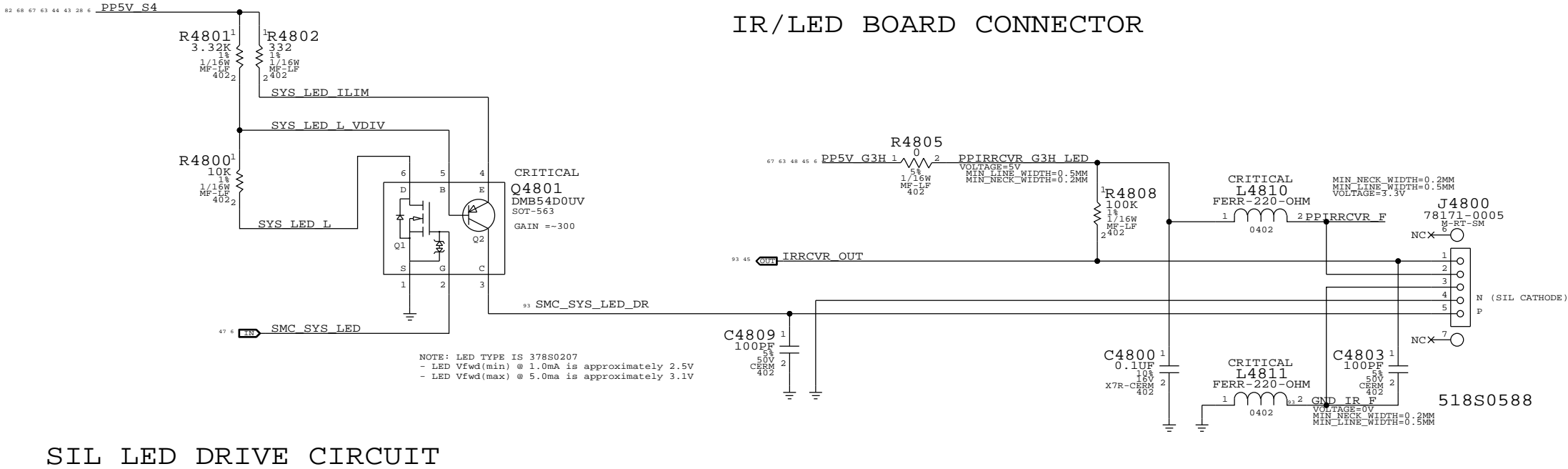
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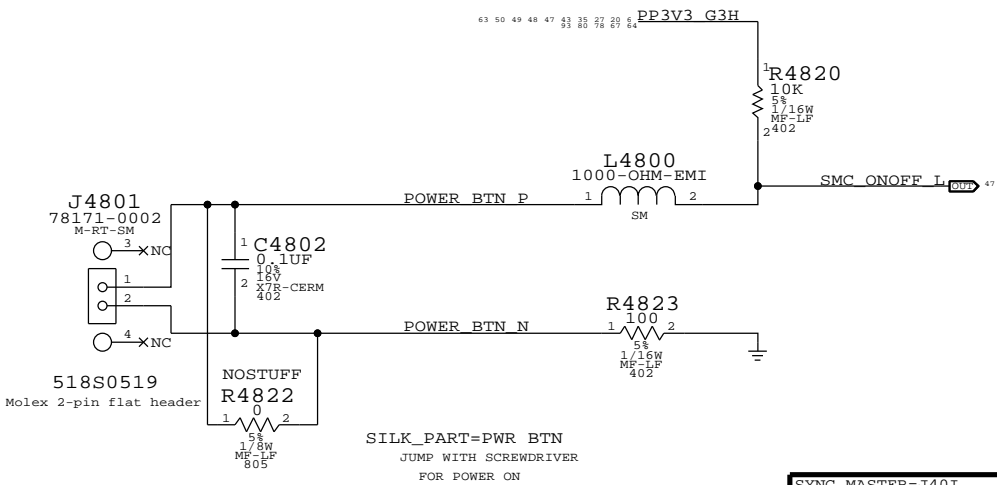
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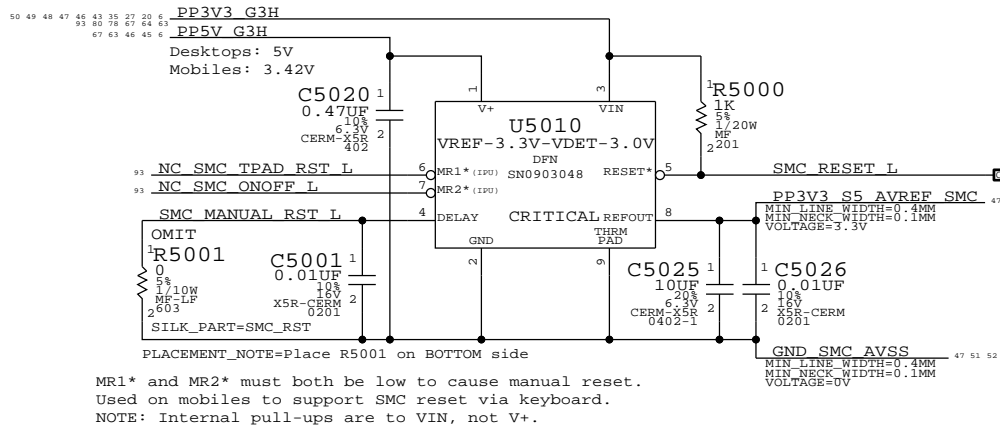


Power Button Header

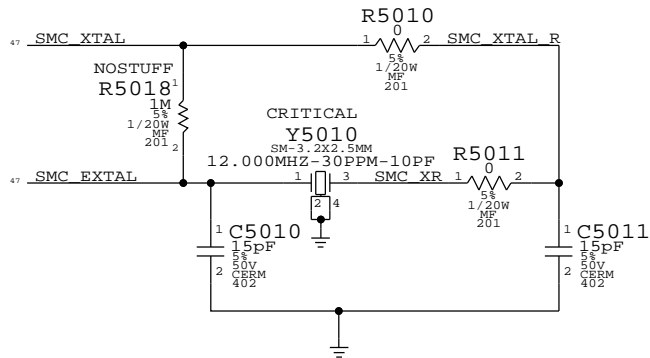


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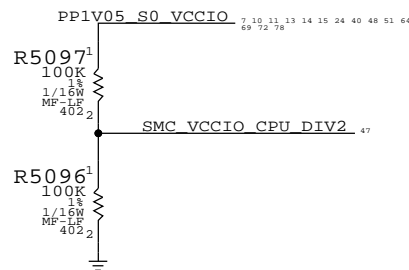
SMC Reset "Button", Supervisor & AVREF Supply



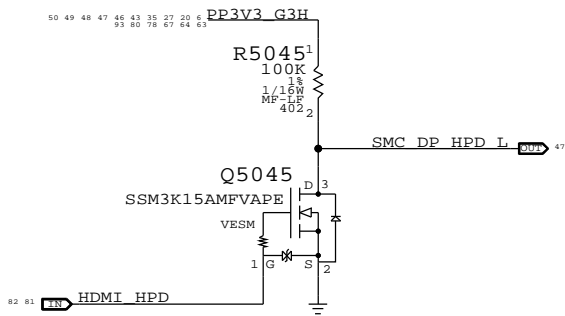
SMC Crystal Circuit



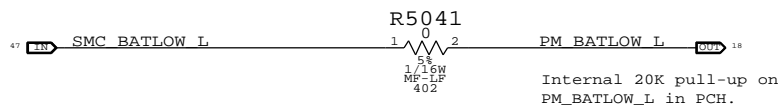
S4 HPD SMC Wake Source



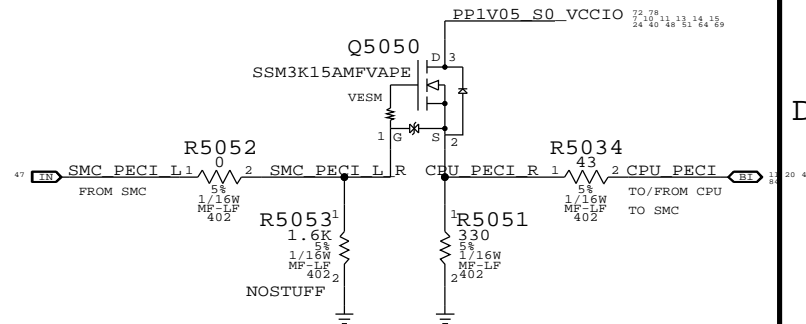
S4 HPD SMC WAKE SOURCES



BATLOW# Isolation

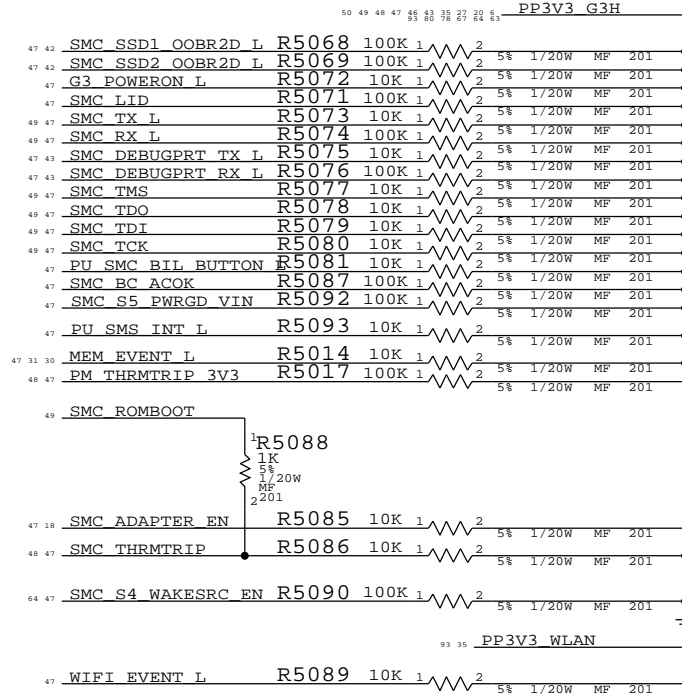
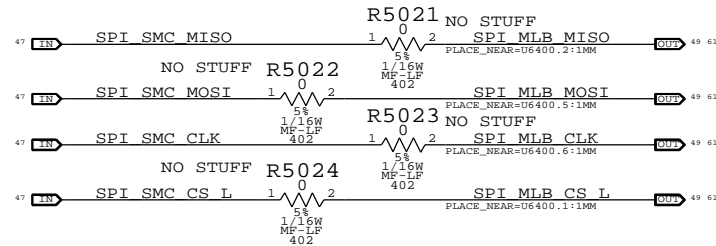


SMC12 Peci Support



SMC12 SPI Support

Series resistors are no stuffed until the topology of 2 SPI Masters are verified.



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SMC Support		DRAWING NUMBER	
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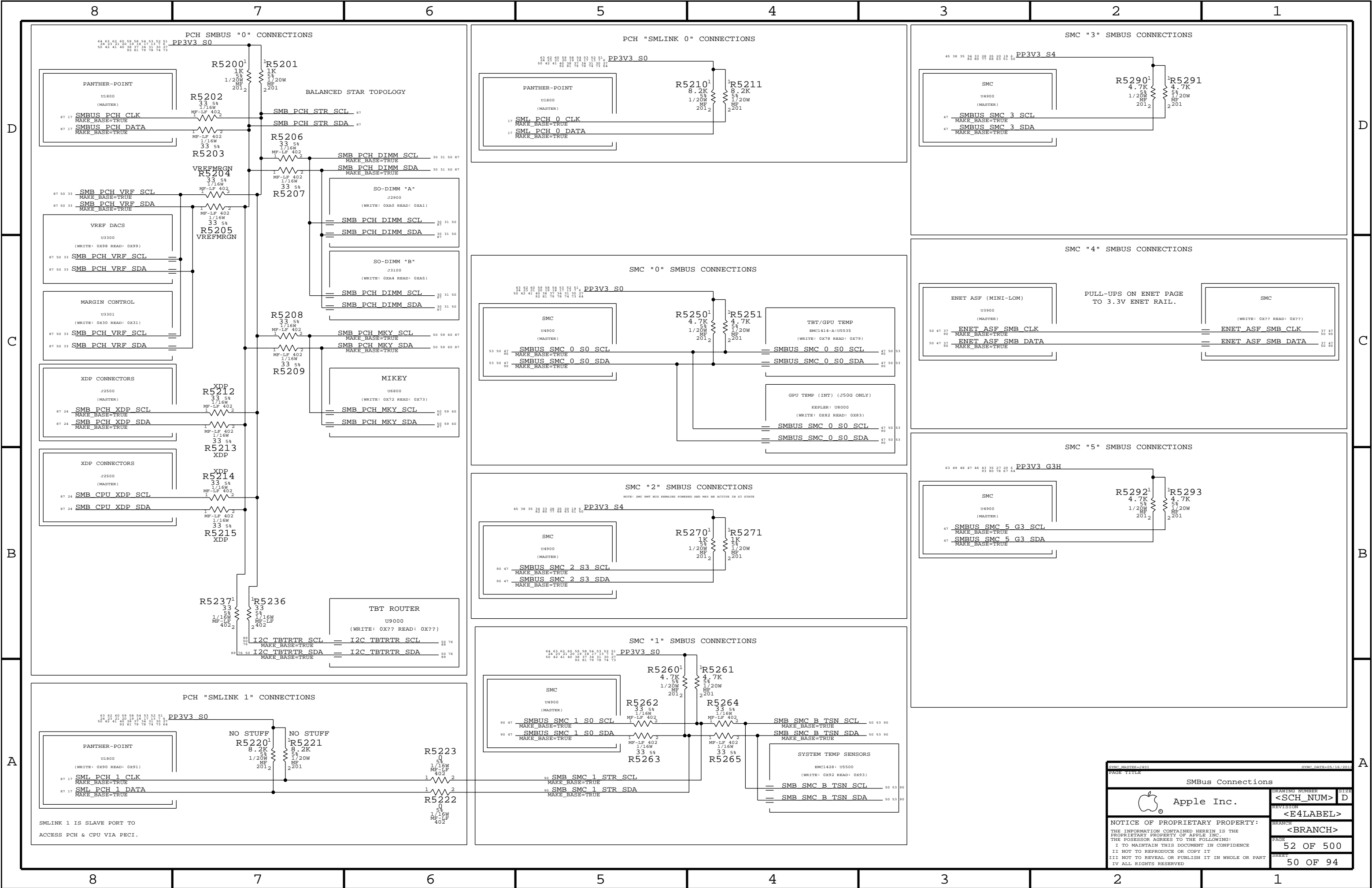



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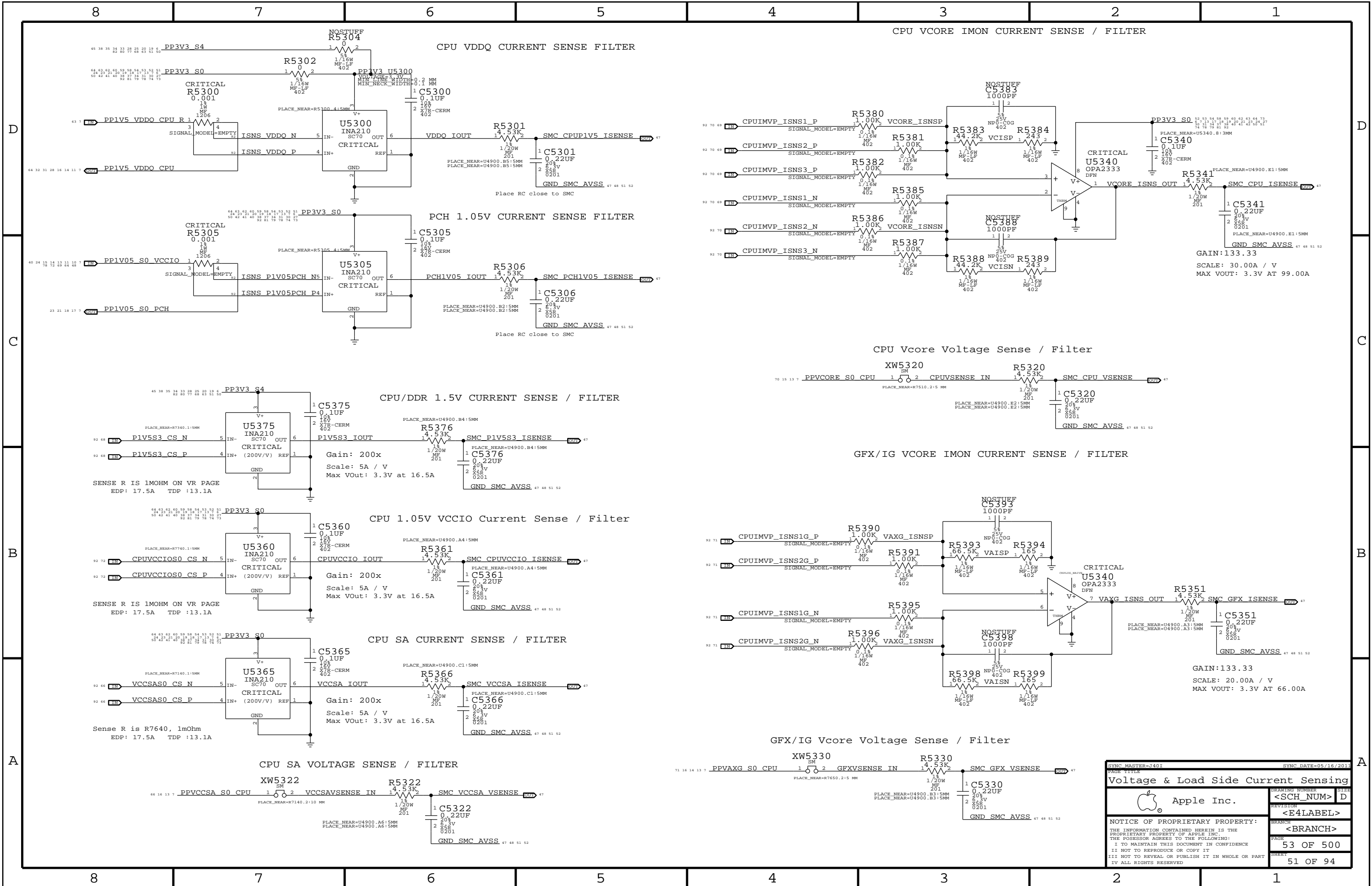
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Voltage & Load Side Current Sensing	
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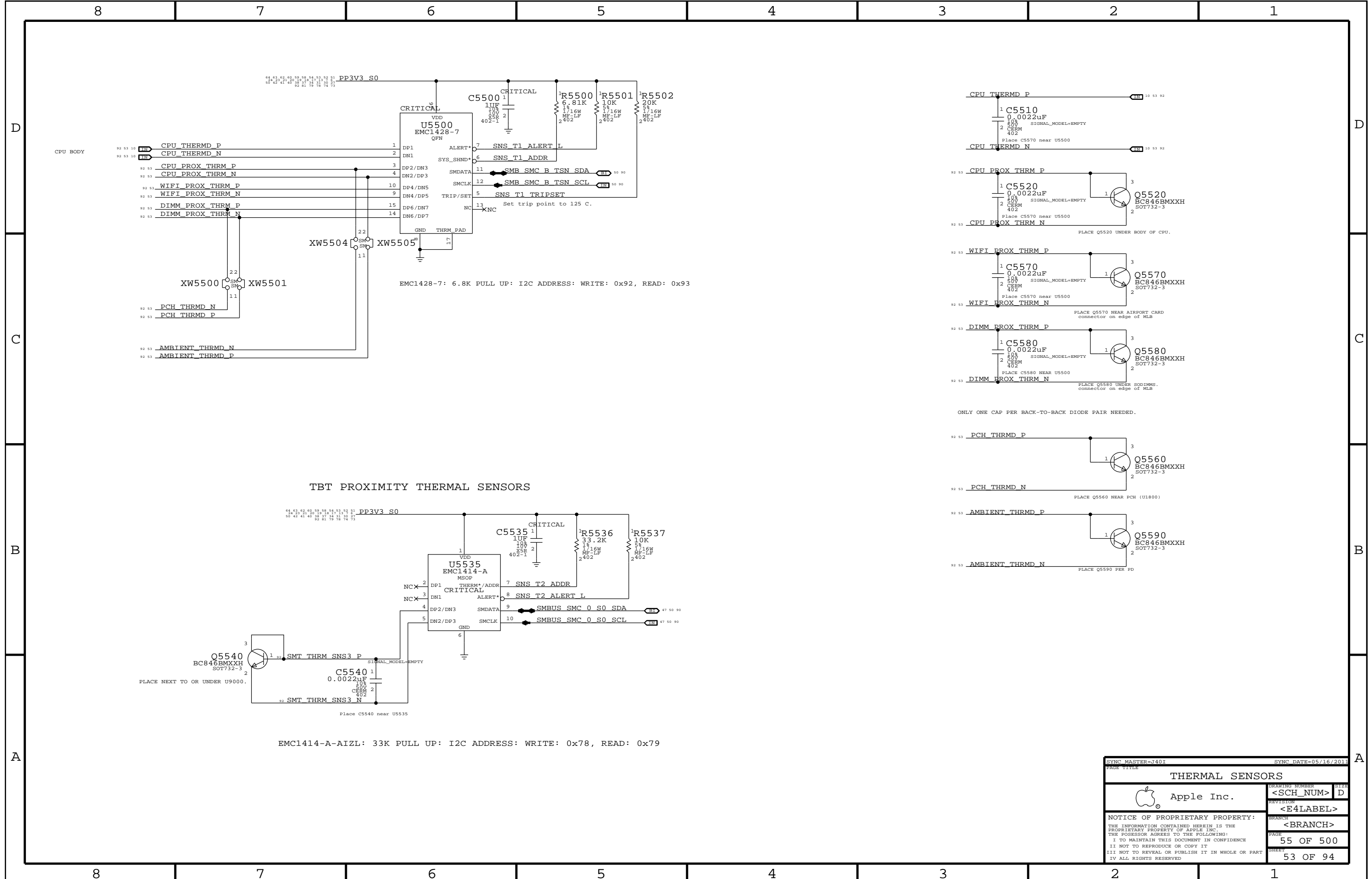



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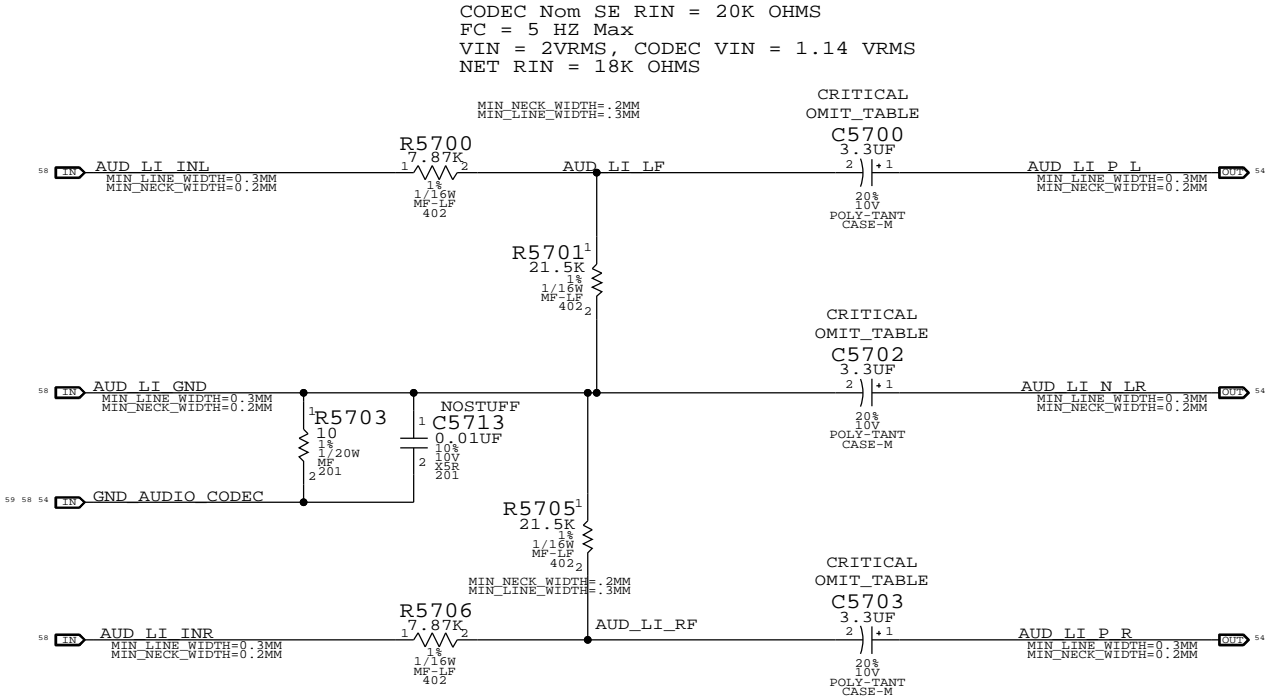
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0309	3	CAP,TANT,POLY,4.7UF,20%,10V,SMD	C5700,C5702,C5703	CRITICAL	?

SYNC_MASTER=J401

SYNC_DATE=05/16/2011

AUDIO:LINE-IN

 Apple Inc.

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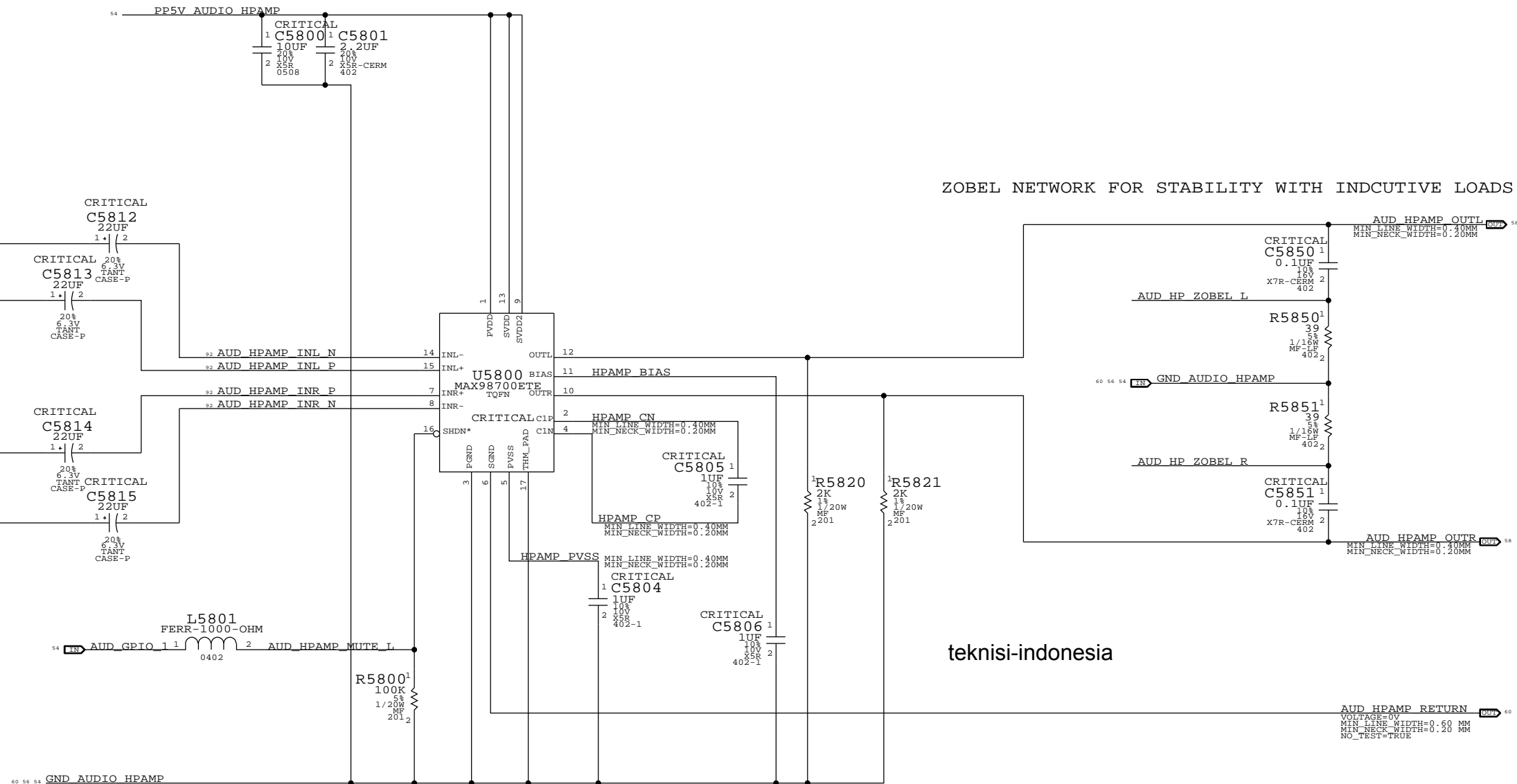
55 OF 94


APN: 353S3244

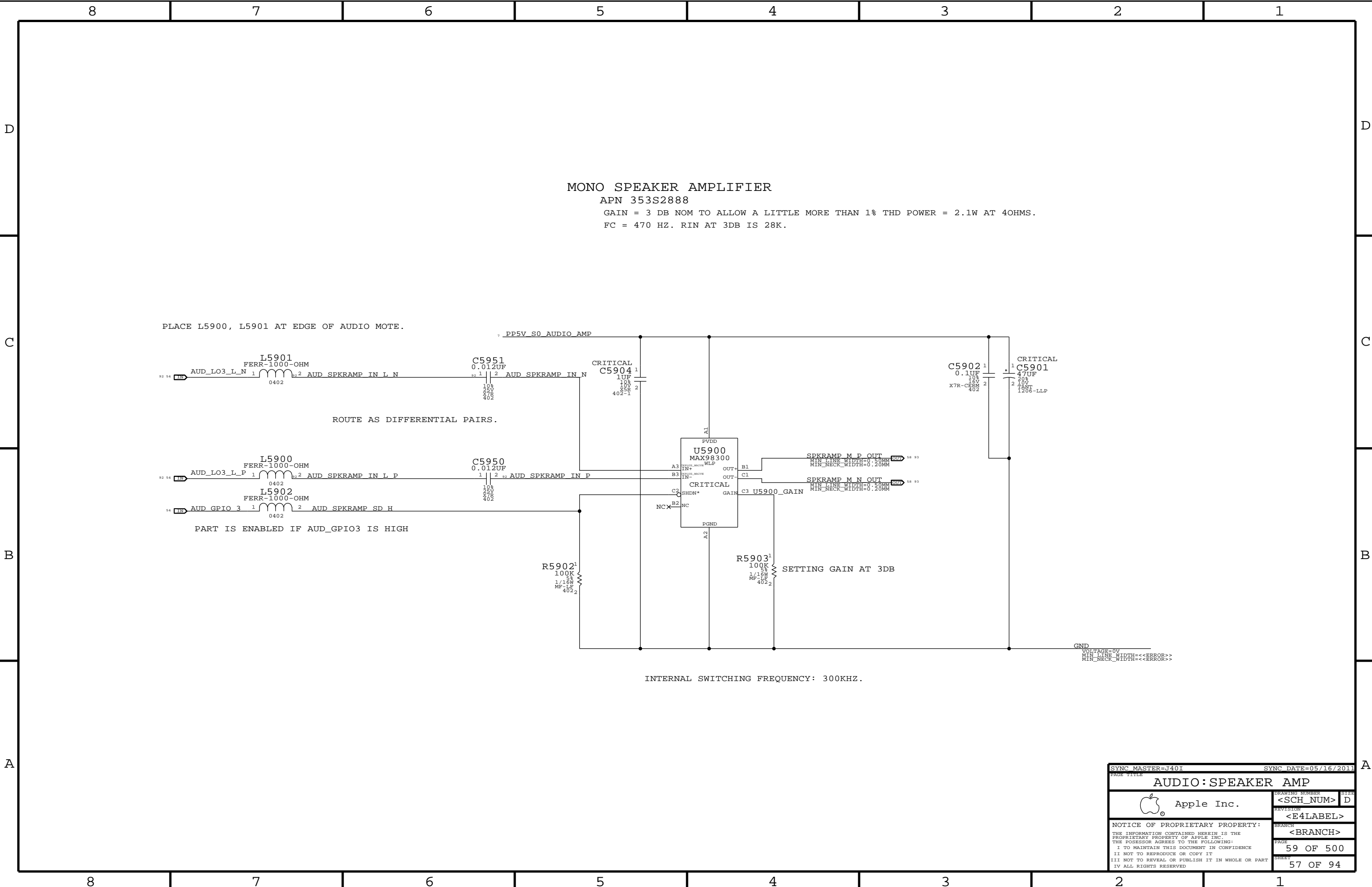
PLACE C5801 NEAR U5800 PIN 9 AND 13


teknisi-indonesia

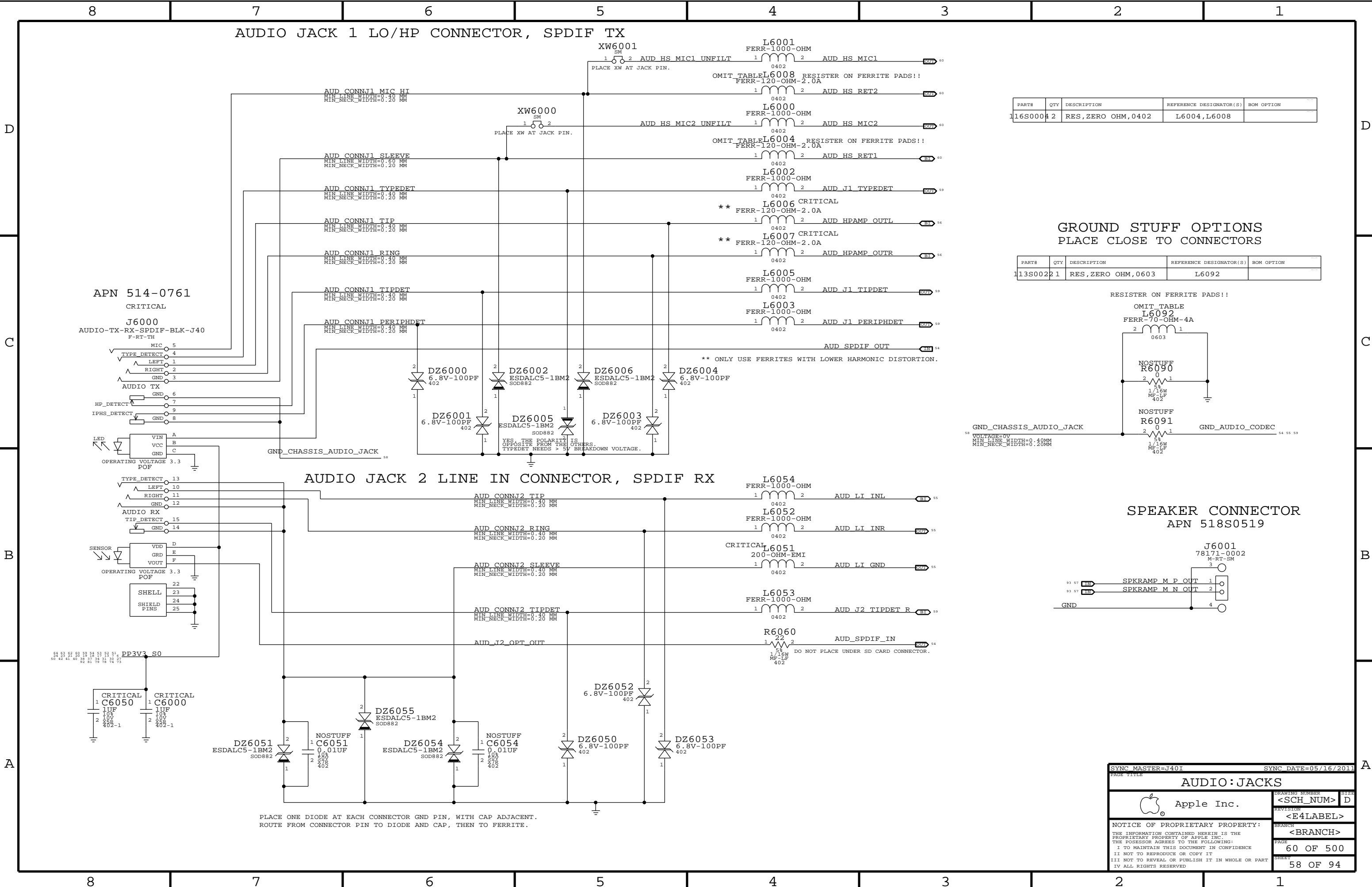
CODEC FILTER STOPBAND:26.256KHZ, ATTENUATION FROM STOPBAND TO 100KHZ IS 102DB



SYMC MASTER=J401		SYMC DATE=05/26/2011	
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SYNC MASTER=J401		SYNC DATE=05/16/2011	
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	PAGE		59 OF 500
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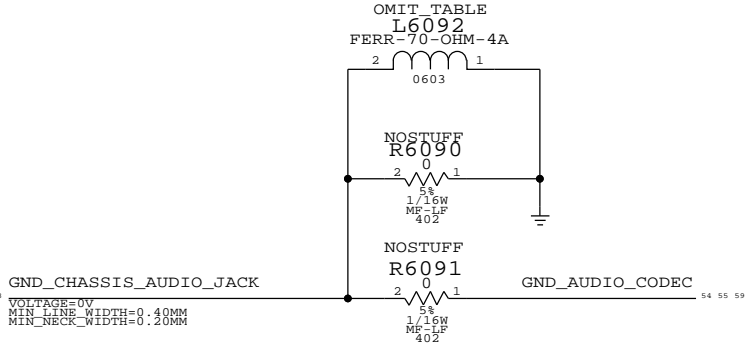


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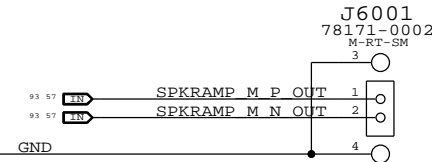
GROUND STUFF OPTIONS
PLACE CLOSE TO CONNECTORS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
113S0022	1	RES,ZERO OHM,0603	L6092	

RESISTER ON FERRITE PADS!!

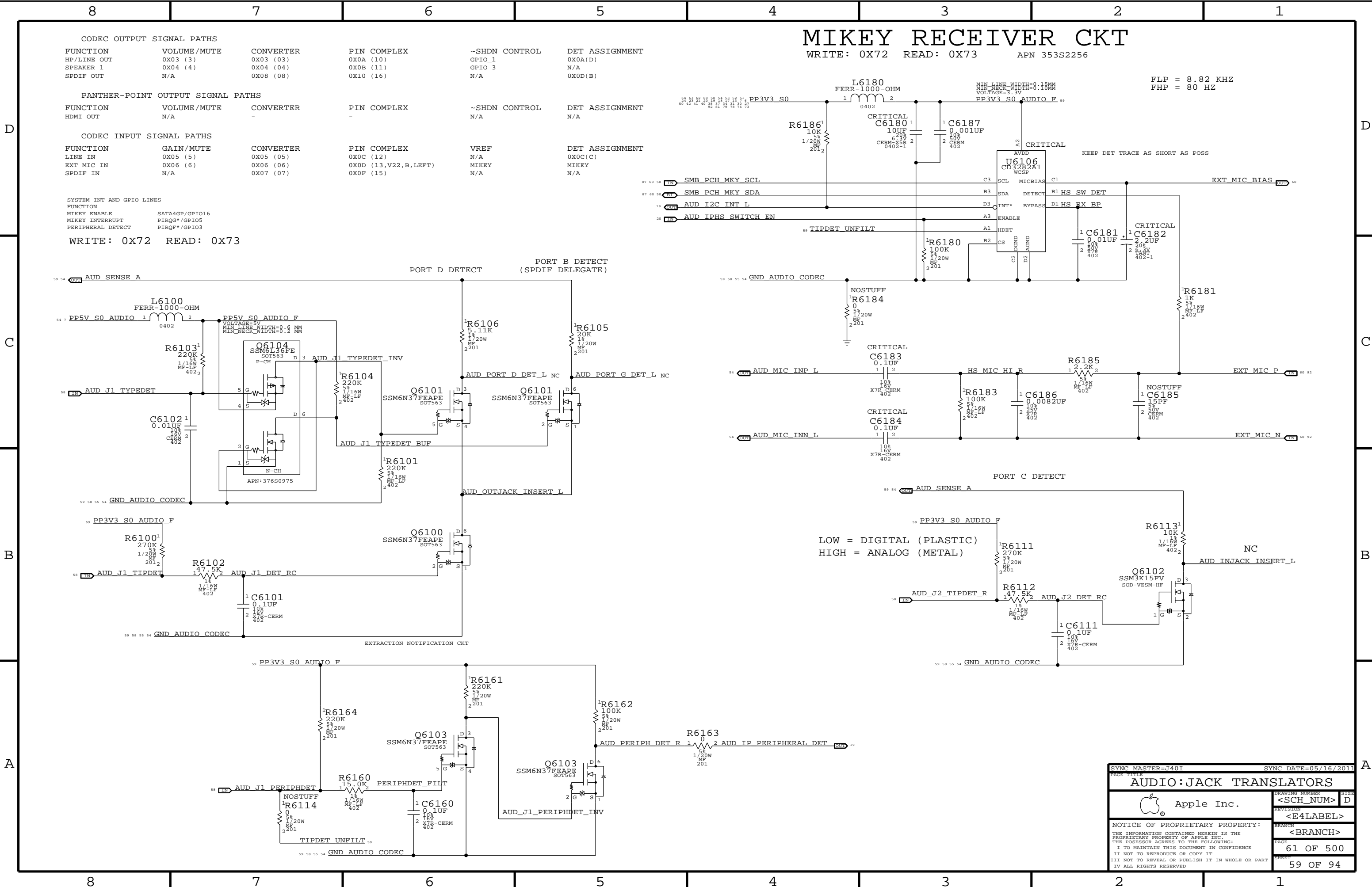


SPEAKER CONNECTOR
APN 518S0519



PLACE ONE DIODE AT EACH CONNECTOR GND PIN, WITH CAP ADJACENT.
ROUTE FROM CONNECTOR PIN TO DIODE AND CAP, THEN TO FERRITE.

PAGE TITLE		SYNC DATE=05/16/2011	
AUDIO:JACKS		DRAWING NUMBER	SIZE
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MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256

FLP = 8.82 KHZ
FHP = 80 HZ

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	~SHDN CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_1	0X0A(D)
SPEAKER 1	0X04 (4)	0X04 (04)	0X0B (11)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (08)	0X10 (16)	N/A	0X0D(B)

PANTHER-POINT OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	~SHDN CONTROL	DET ASSIGNMENT
HDMI OUT	N/A	-	-	N/A	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	GAIN/MUTE	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X05 (05)	0X0C (12)	N/A	0X0C(C)
EXT MIC IN	0X06 (6)	0X06 (06)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY
SPDIF IN	N/A	0X07 (07)	0X0F (15)	N/A	N/A

SYSTEM INT AND GPIO LINES

FUNCTION	
MIKEY ENABLE	SATA4GP/GPIO16
MIKEY INTERRUPT	PIRQG*/GPIO5
PERIPHERAL DETECT	PIRQF*/GPIO3

WRITE: 0X72 READ: 0X73

PORT D DETECT

PORT B DETECT (SPDIF DELEGATE)

PORT C DETECT

LOW = DIGITAL (PLASTIC)
HIGH = ANALOG (METAL)

SYNC MASTER=J401		SYNC DATE=05/16/2011	
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AUDIO:JACK TRANSLATORS		<SCH_NUM>	
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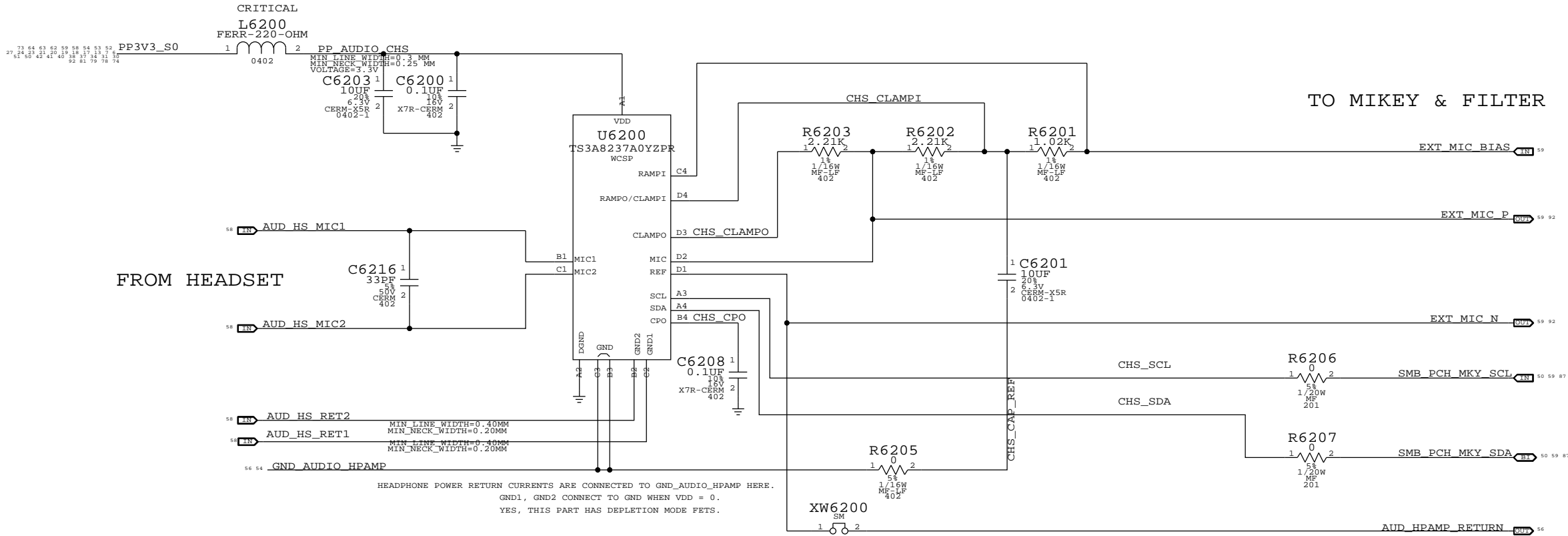
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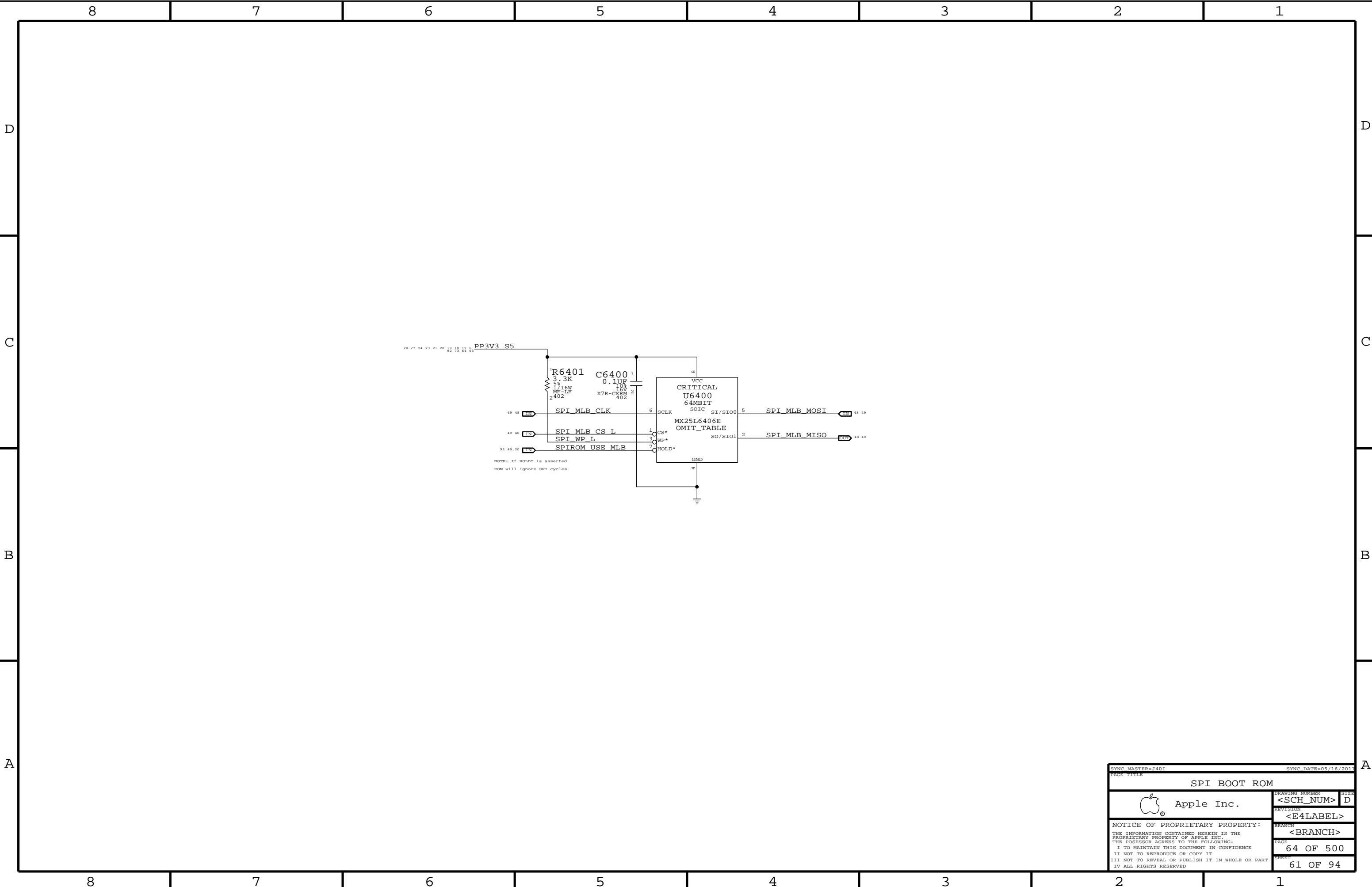
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EXTERNAL (HEADSET) MIC INPUT CIRCUITRY APN:353S3522



I2C ADDRESSES: CHS uses SMBus 0 connections

CHS	U6200	READ	0111	0111	0X77
CHS	U6200	WRITE	0111	0110	0X76

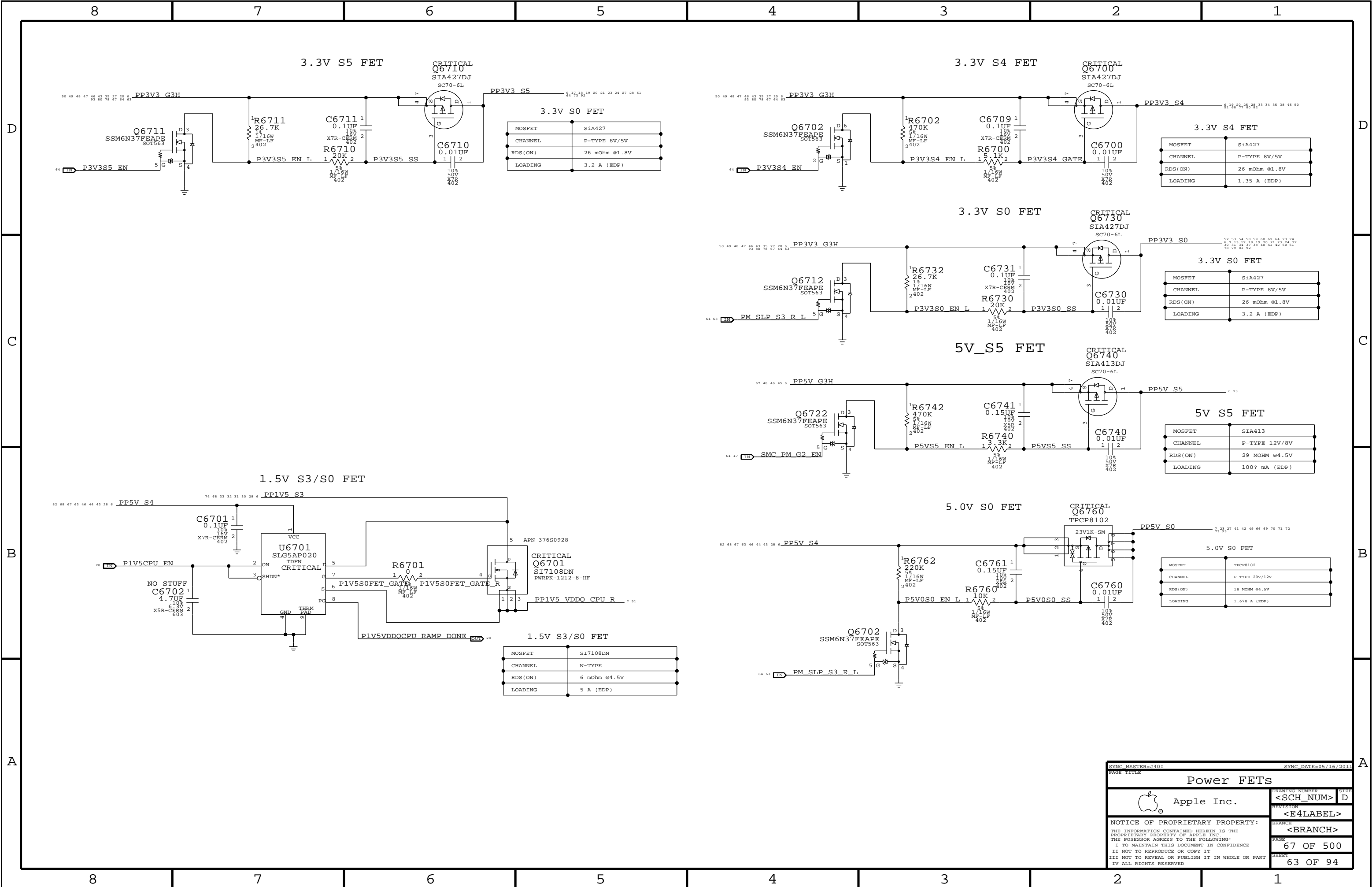


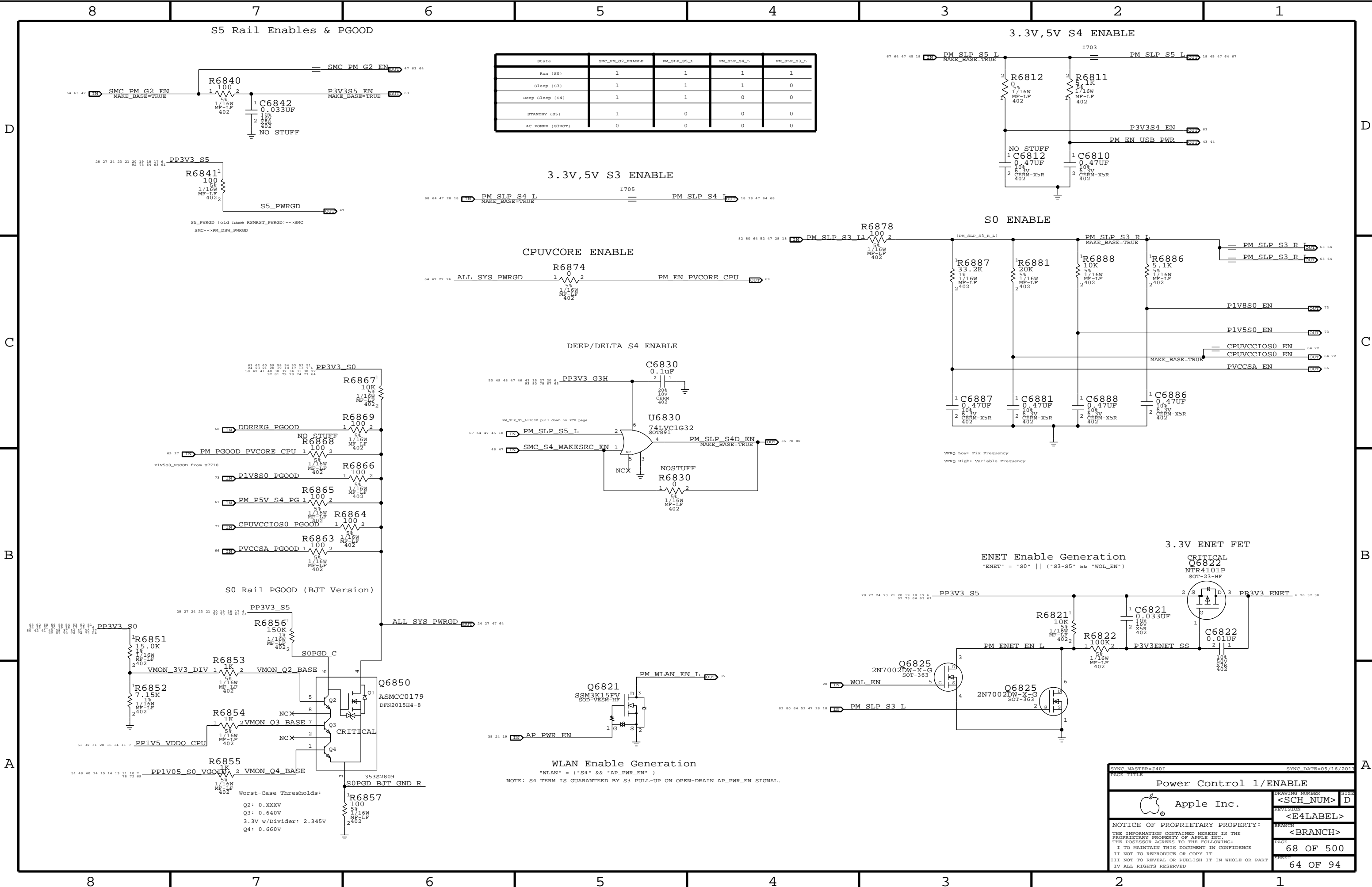
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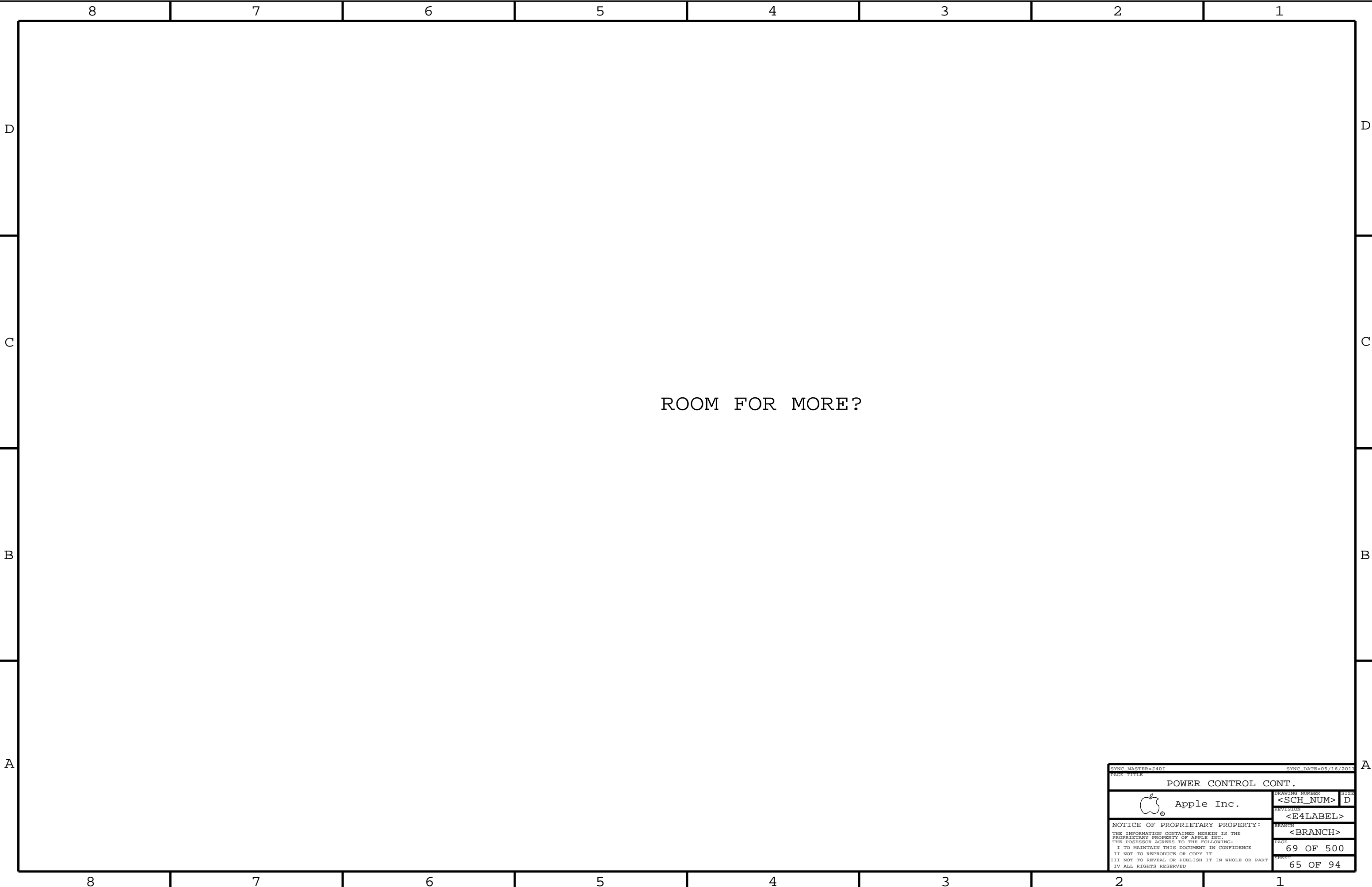
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State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
STANDBY (S5)	1	0	0	0
AC POWER (G3NOT)	0	0	0	0

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
STANDBY (S5)	1	0	0	0
AC POWER (G3NOT)	0	0	0	0




SYNC MASTER=J40I

SYNC DATE=05/16/2011

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POWER CONTROL CONT.

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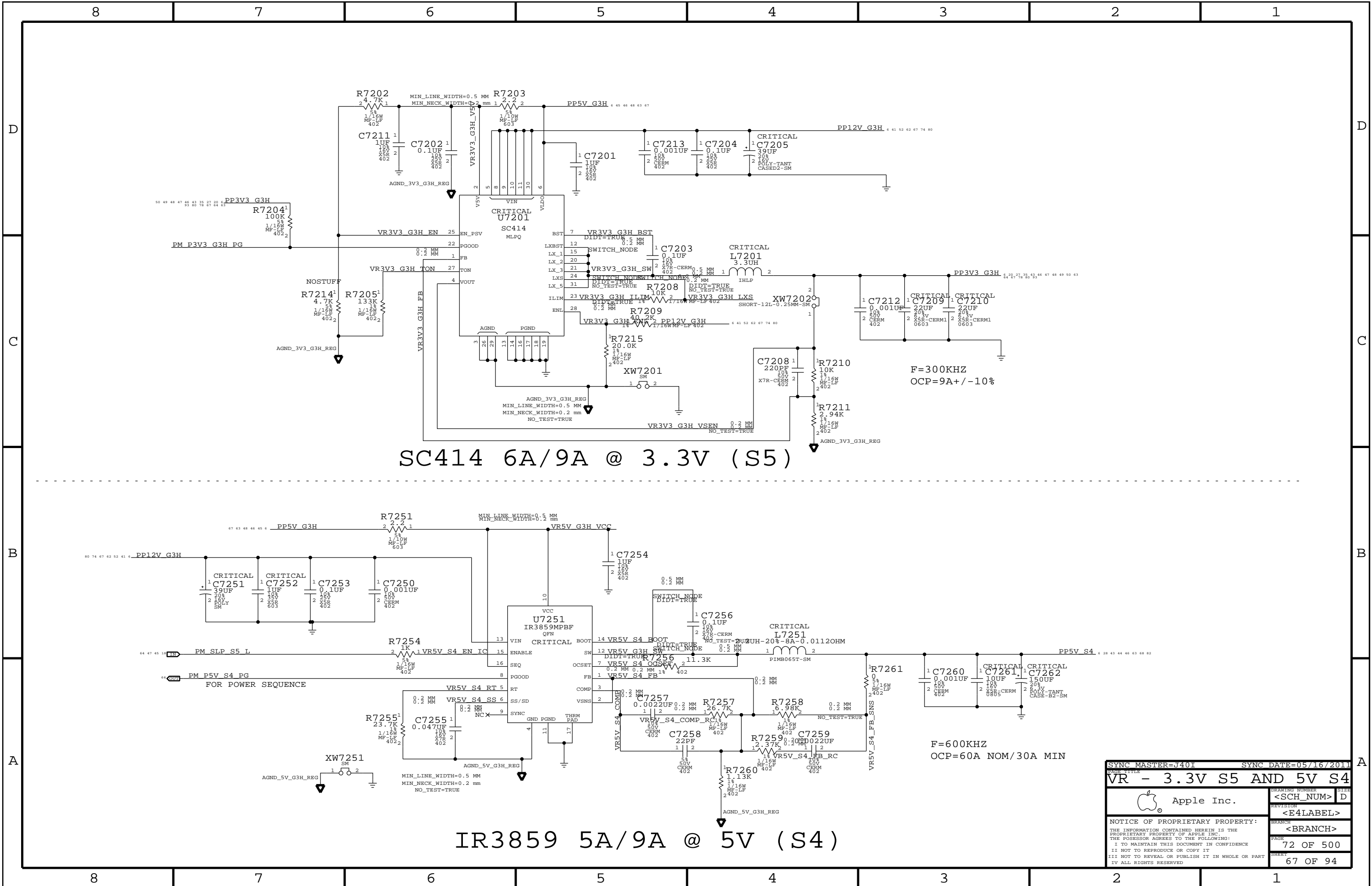
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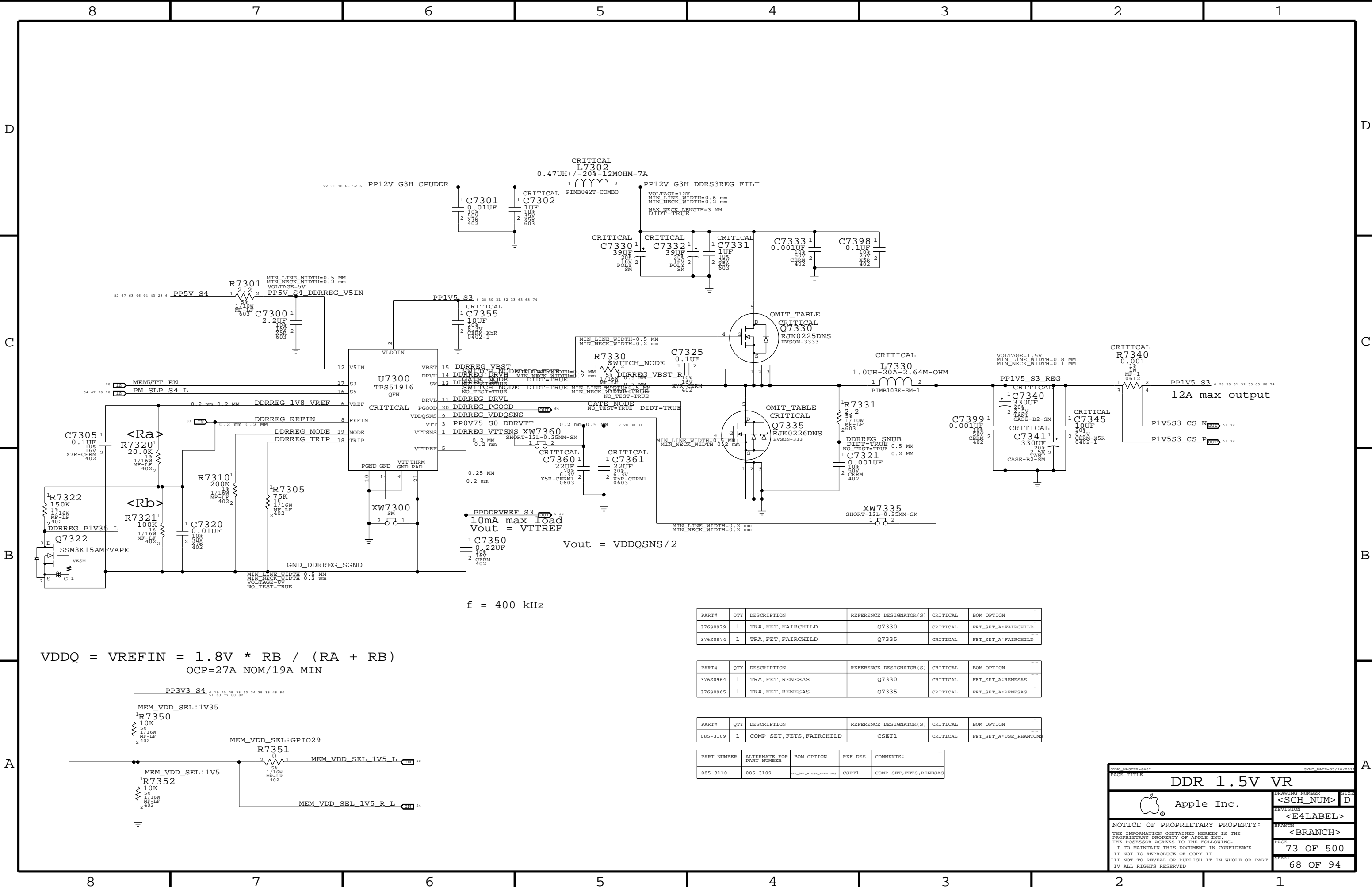
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SC414 6A/9A @ 3.3V (S5)

IR3859 5A/9A @ 5V (S4)

SYNC MASTER=J401		SYNC DATE=05/16/2011	
VR - 3.3V S5 AND 5V S4			
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$$VDDQ = VREFIN = 1.8V * RB / (RA + RB)$$

$$OCp=27A \text{ NOM}/19A \text{ MIN}$$

f = 400 kHz

Vout = VDDQSNS/2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0979	1	TRA,FET,FAIRCHILD	Q7330	CRITICAL	FET_SET_A:FAIRCHILD
376S0874	1	TRA,FET,FAIRCHILD	Q7335	CRITICAL	FET_SET_A:FAIRCHILD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0964	1	TRA,FET,RENESAS	Q7330	CRITICAL	FET_SET_A:RENESAS
376S0965	1	TRA,FET,RENESAS	Q7335	CRITICAL	FET_SET_A:RENESAS


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
085-3109	1	COMP SET,FETS,FAIRCHILD	CSET1	CRITICAL	FET_SET_A:USE_PHANTOMS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
085-3110	085-3109	FET_SET_A:USE_PHANTOMS	CSET1	COMP SET,FETS,RENESAS

SYDC PART#-3401

SYDC DATE=05/16/2011

DDR 1.5V VR

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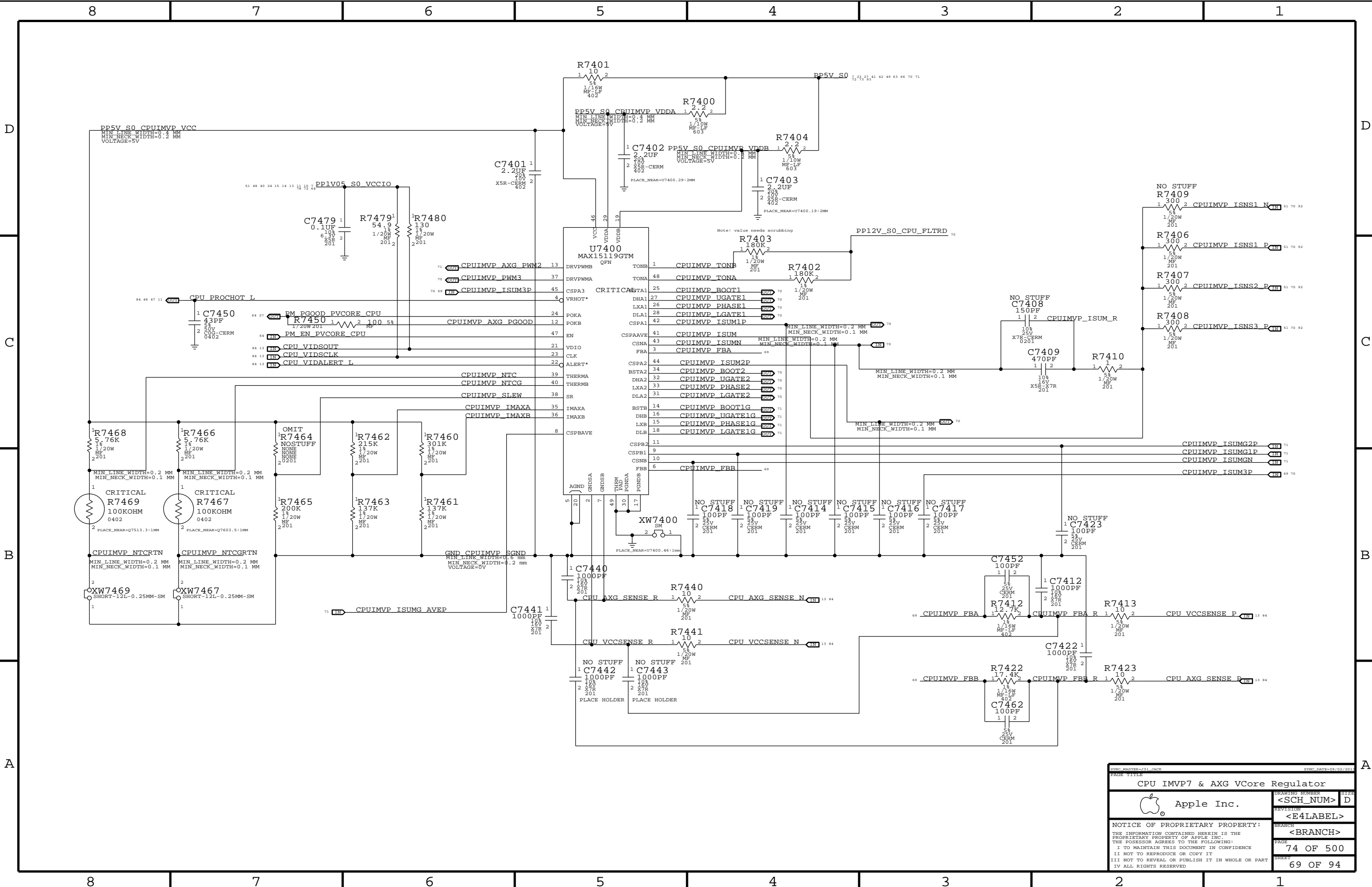
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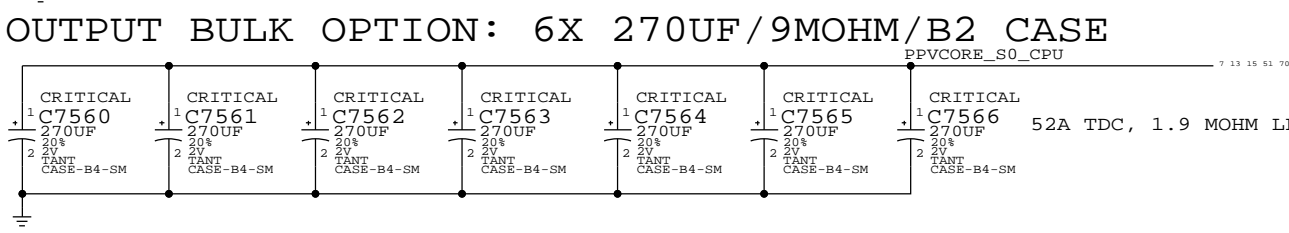
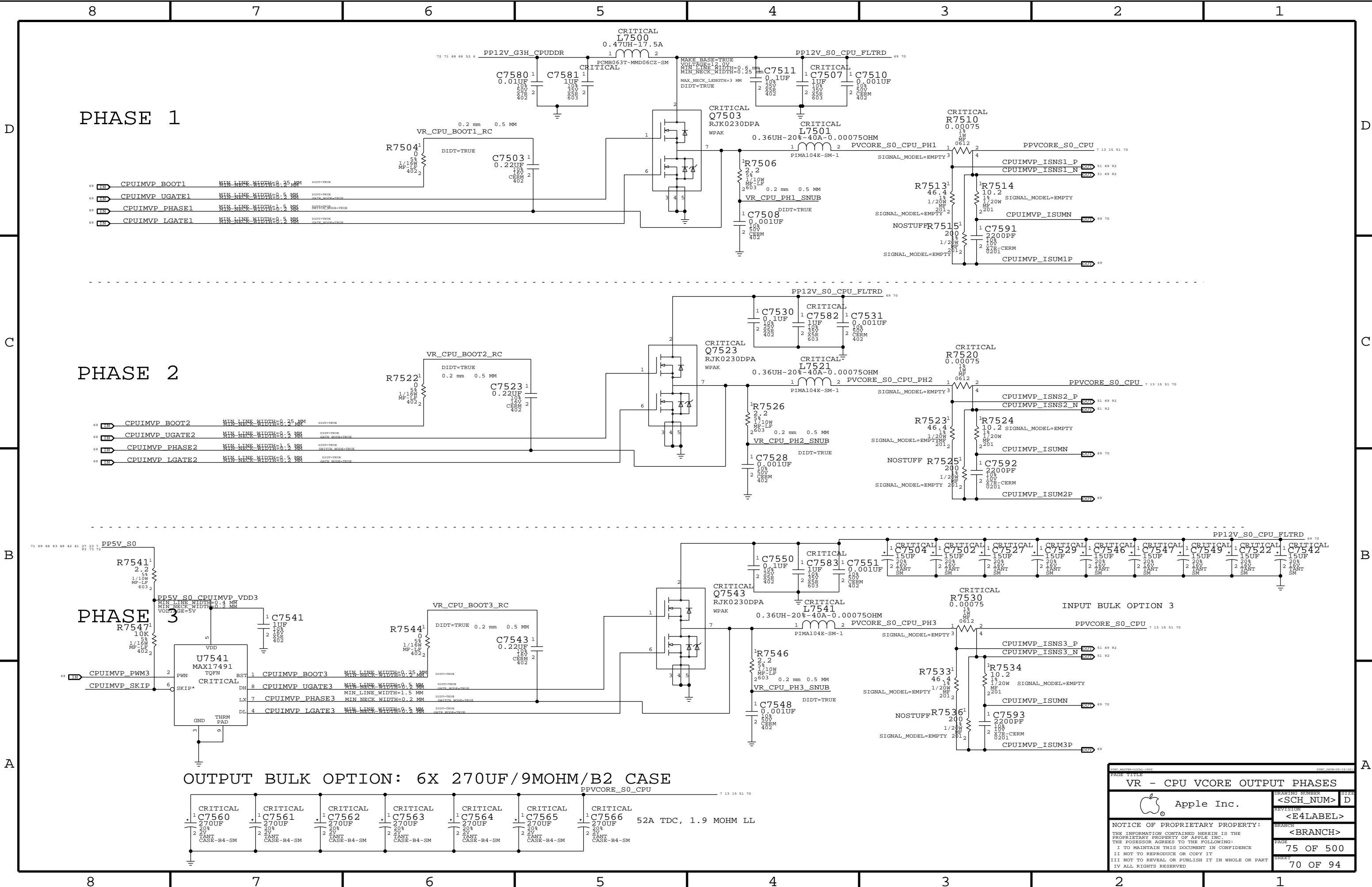
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SYDC MASTER-111 - 0000		SYDC DATE=09/03/2011	
PAGE TITLE			
CPU IMVP7 & AXG VCore Regulator			
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VR - CPU VCore OUTPUT PHASES	
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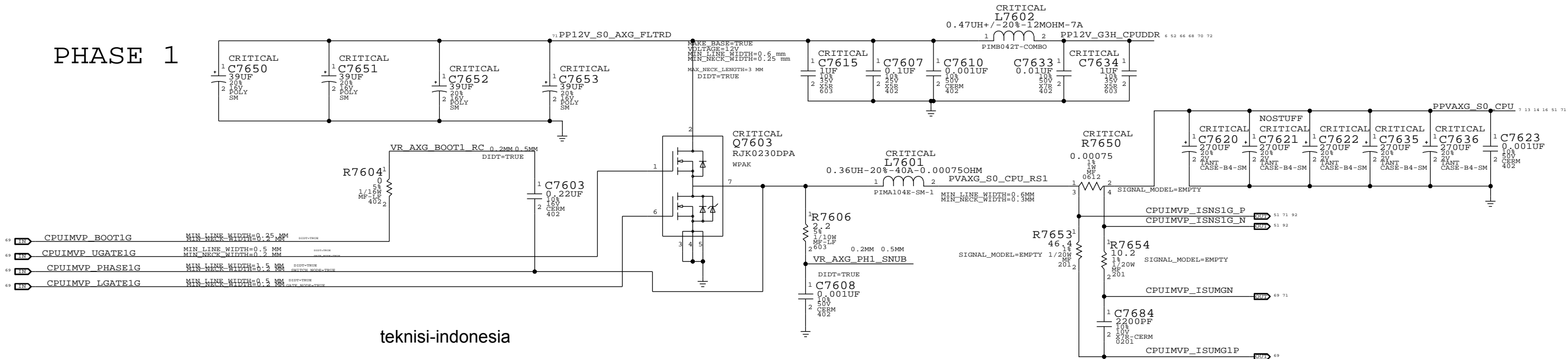
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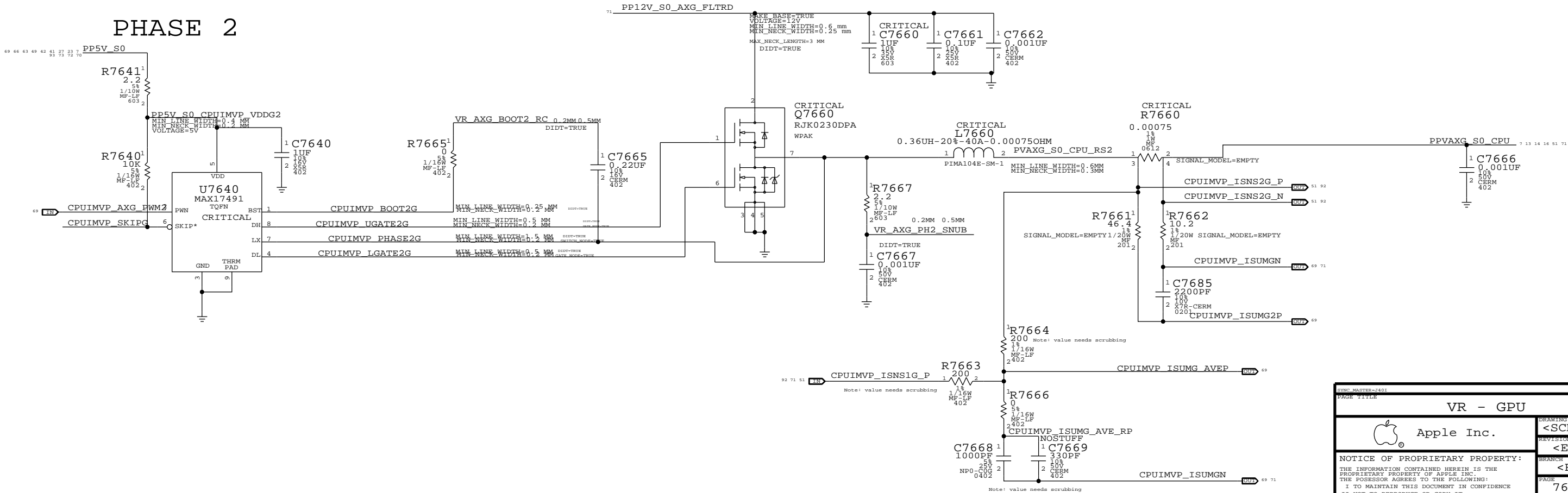
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AXG PHASE (35A AVG/50A PEAK, 3.9MOHM LL)

PHASE 1



PHASE 2



VR - GPU

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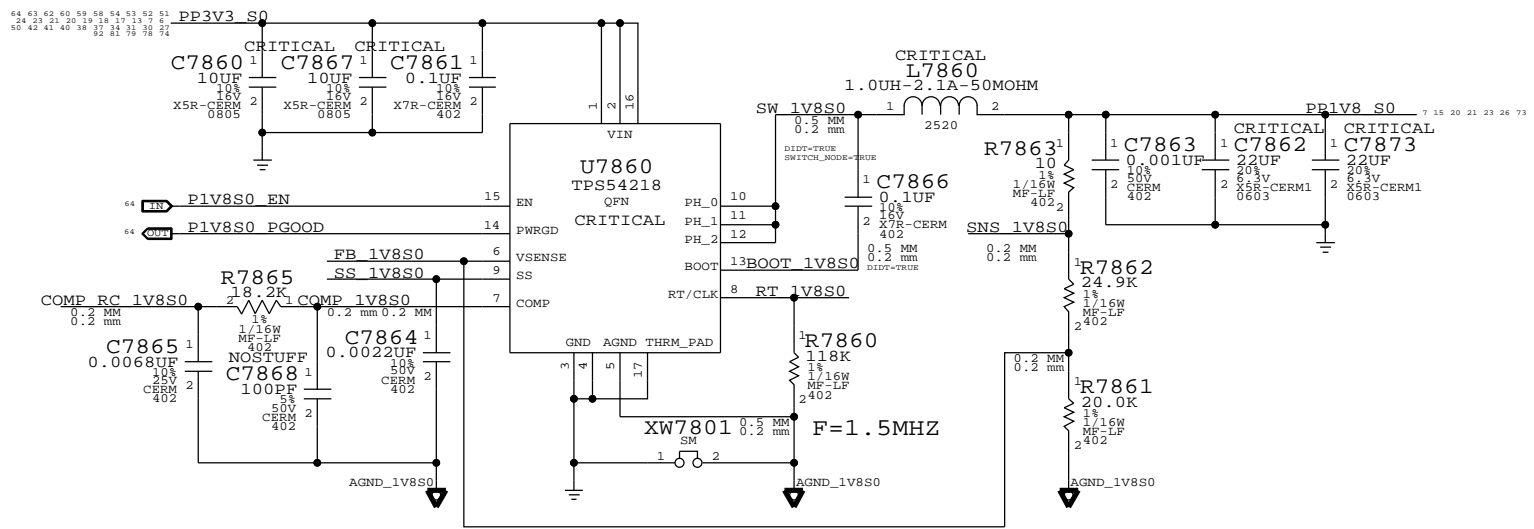
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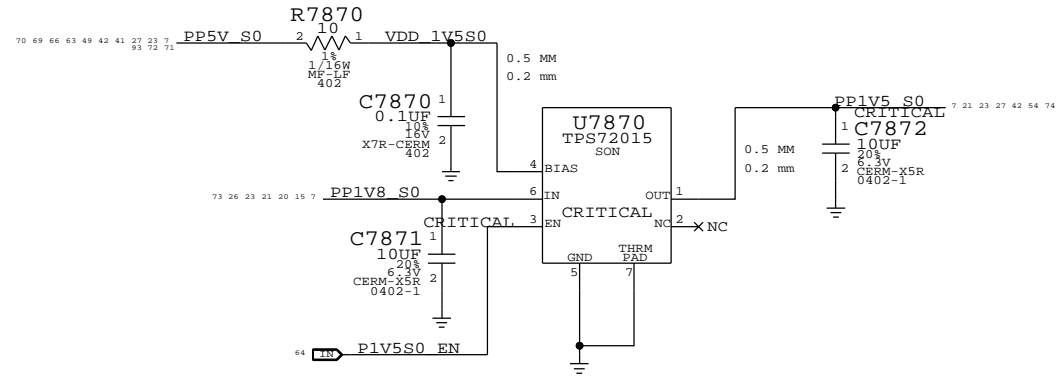
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1.8V S0 SWITCHER @ 1.7A/2A

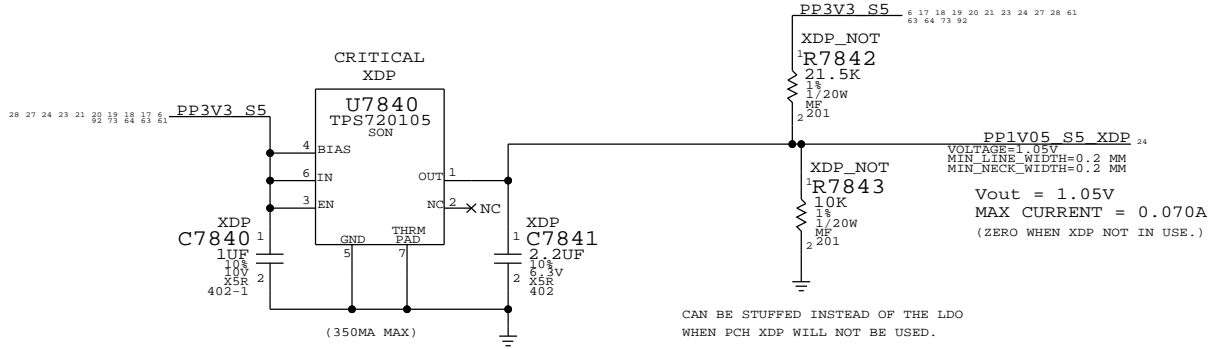


1.5V S0 @ 0.3A/0.5A

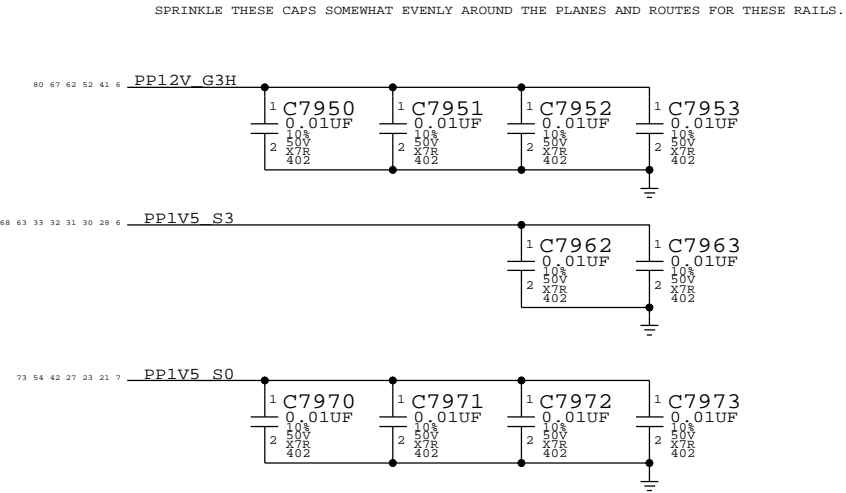
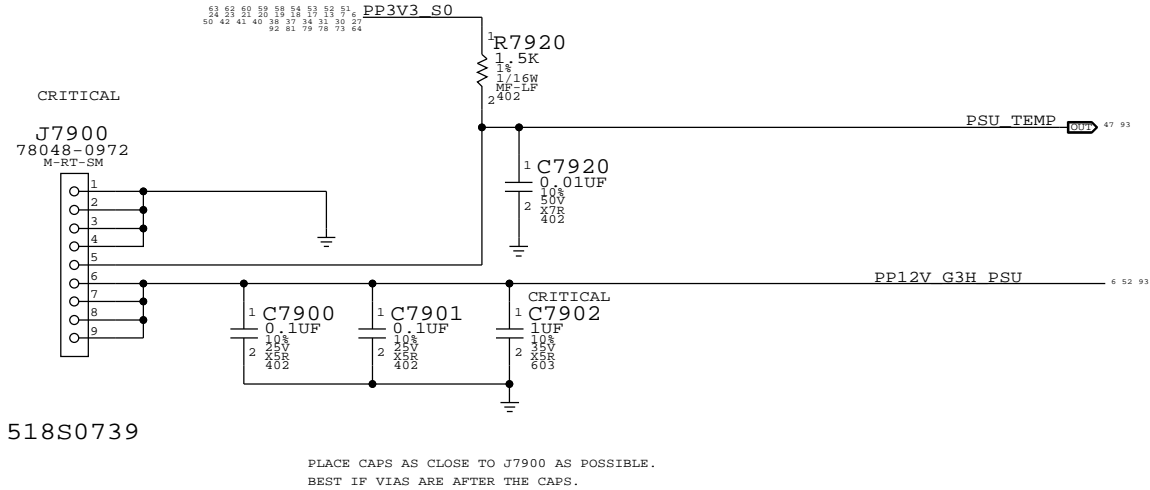
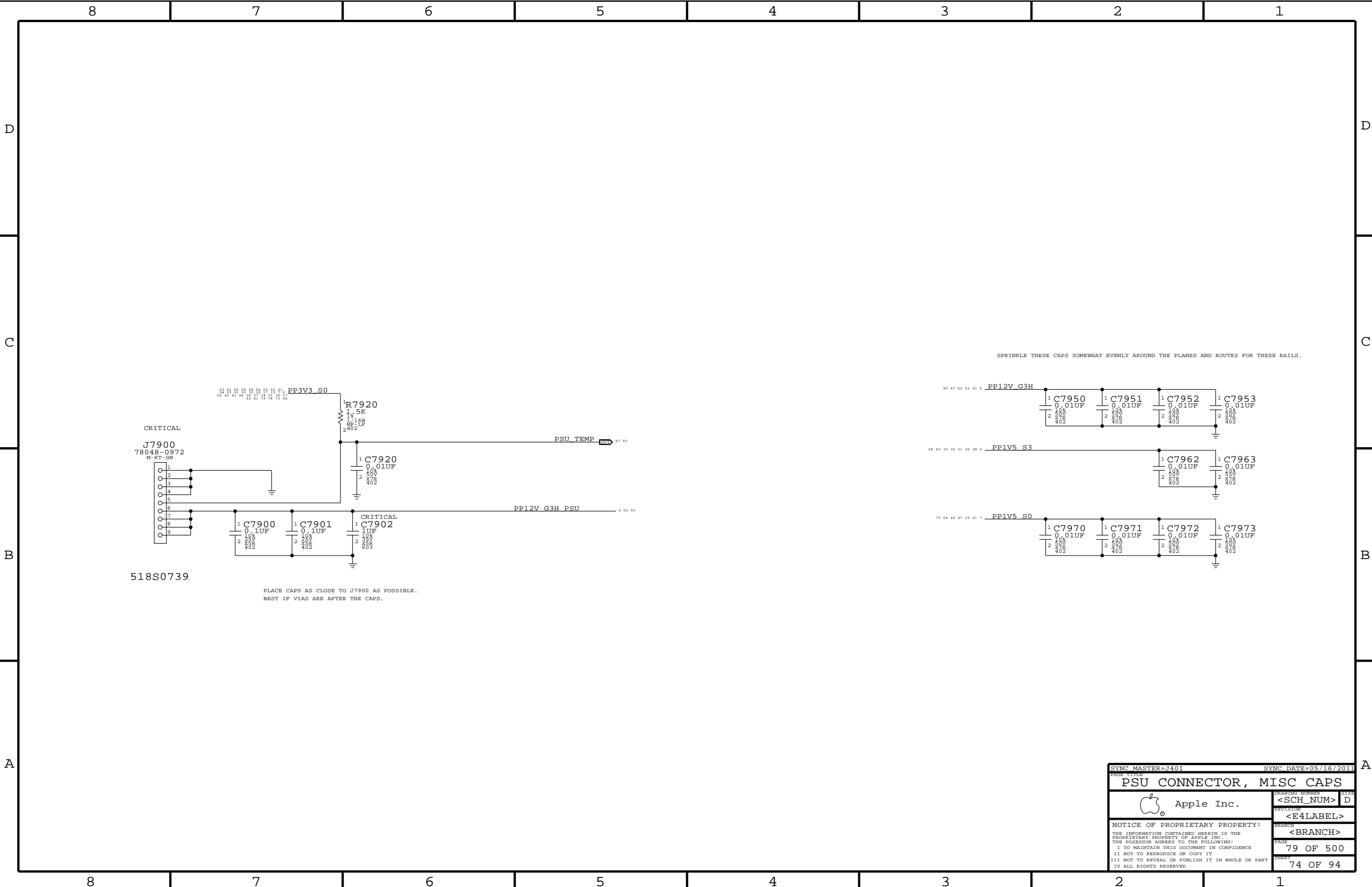



1.05V S5 XDP LDO

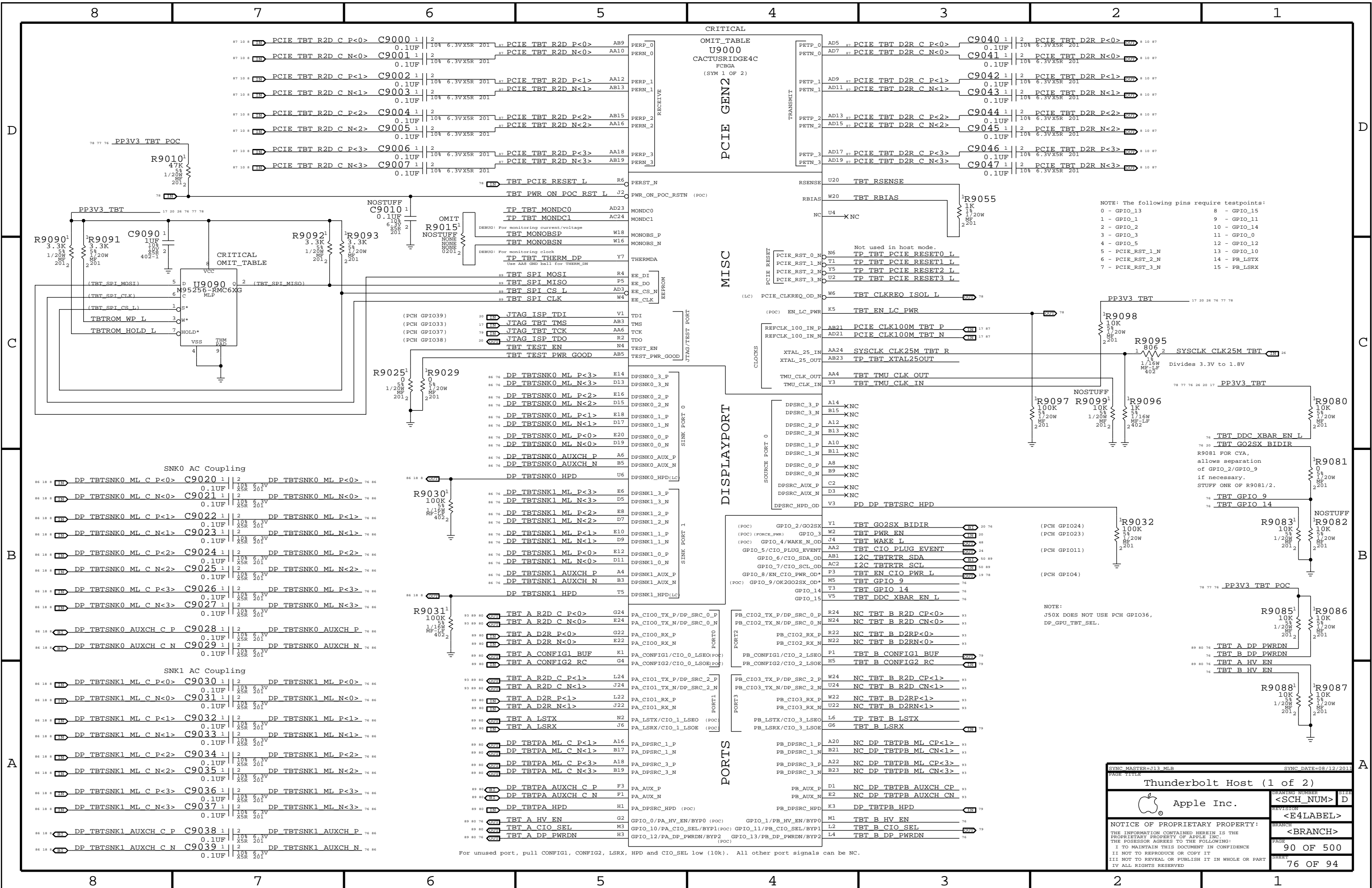
PANTHER-POINT REQUIRES JTAG PULL-UPS TO BE POWERED AT 1.05V WHEN SUS SUSPEND WELL IS ACTIVE. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

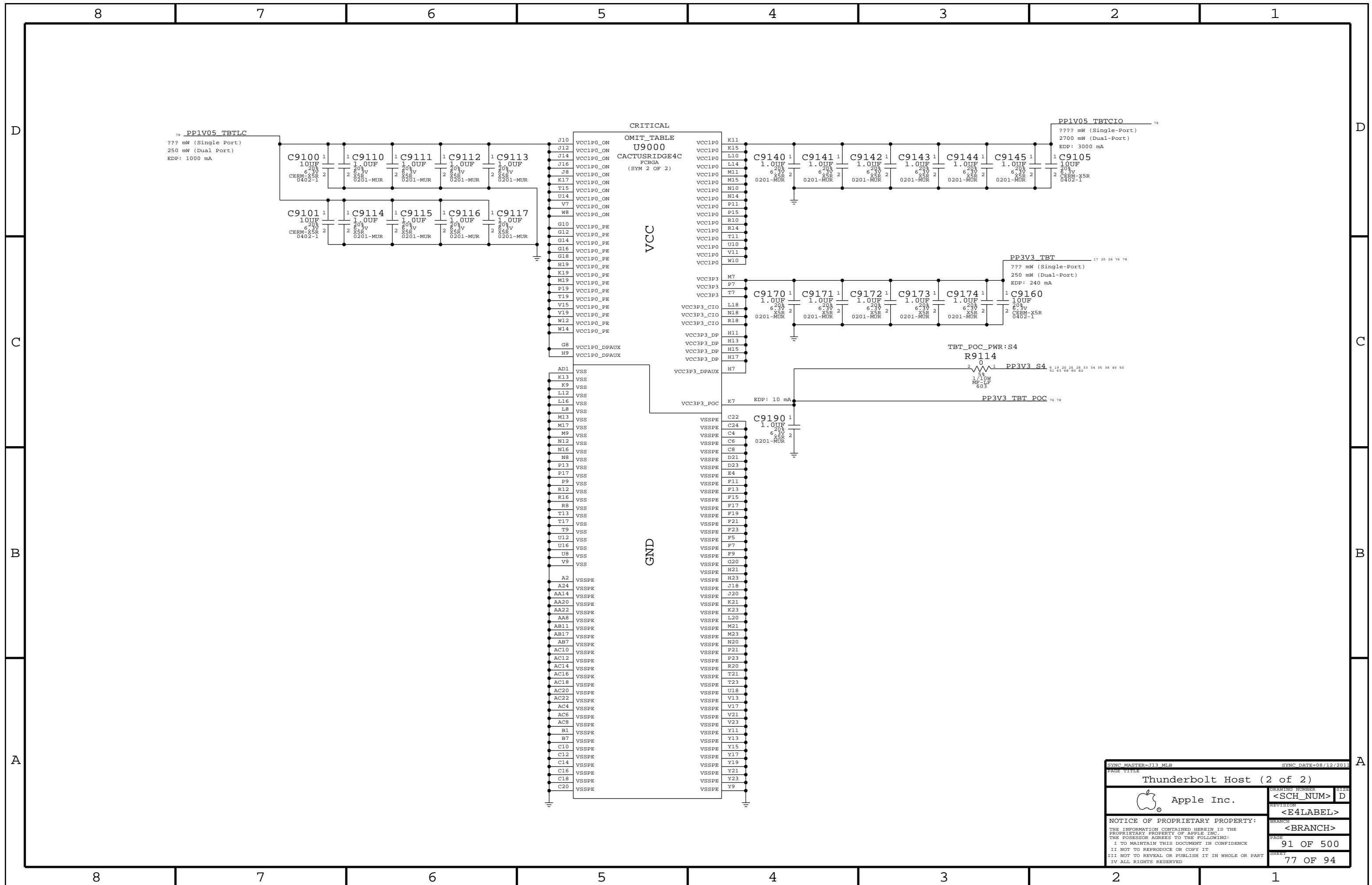


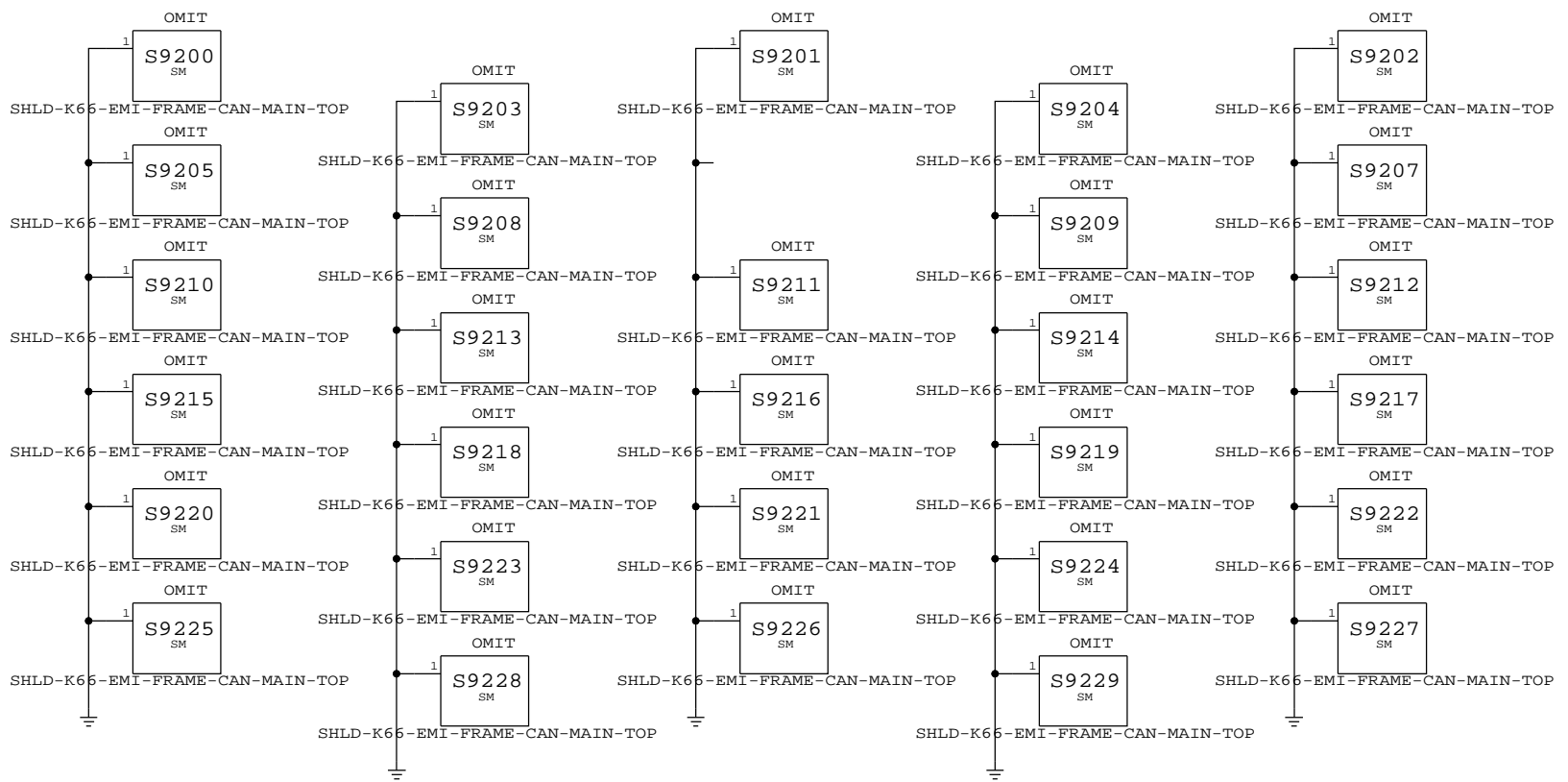
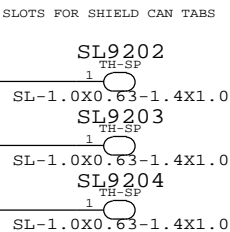
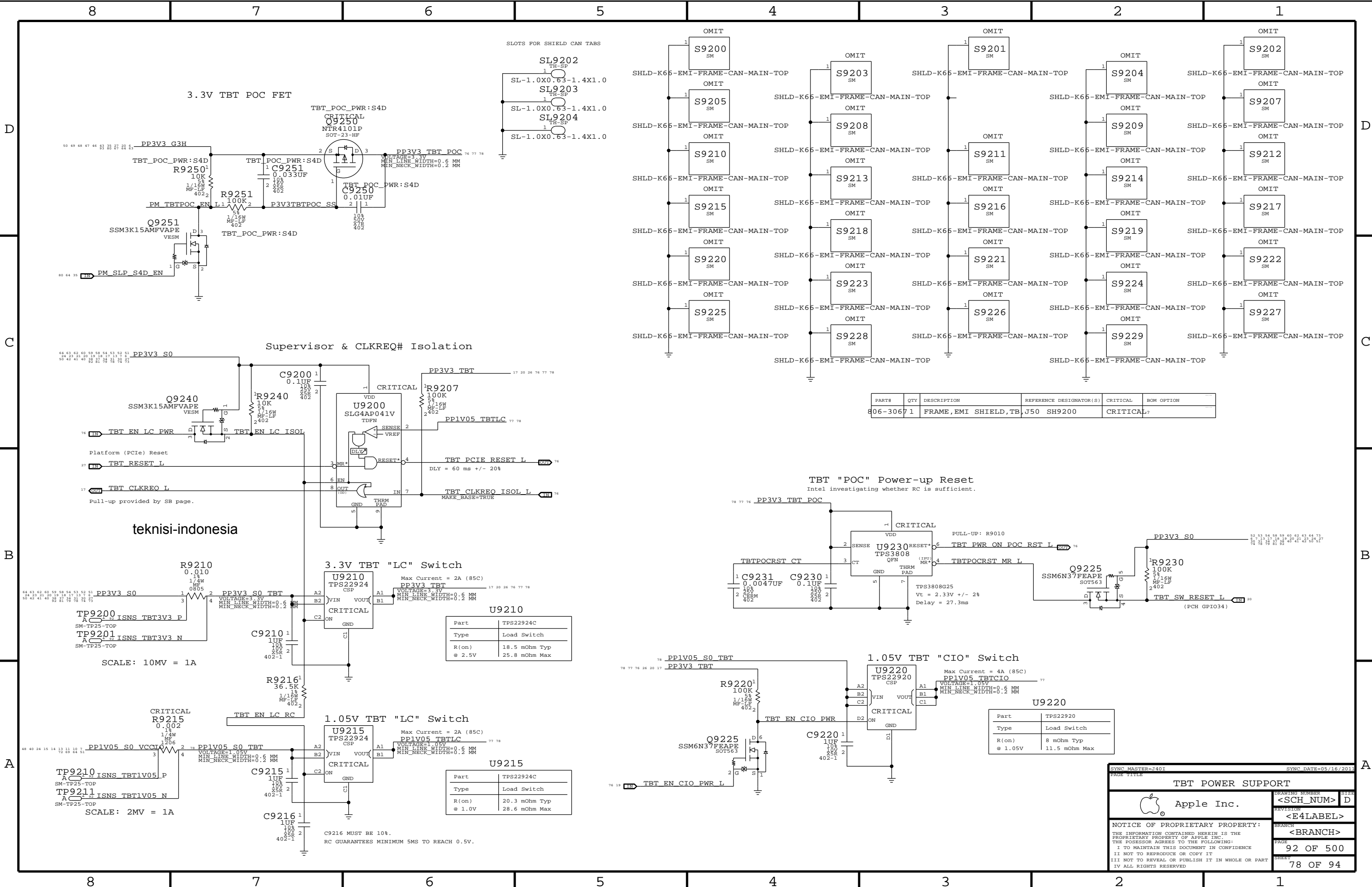
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PSU CONNECTOR, MISC CAPS			
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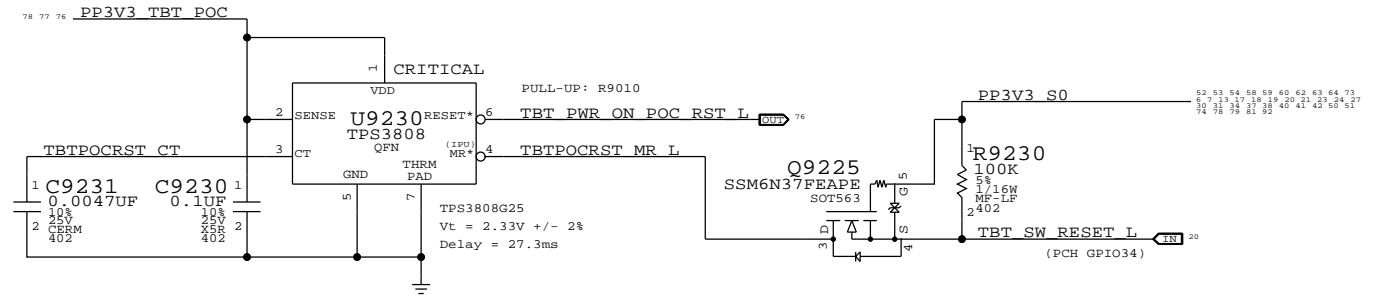




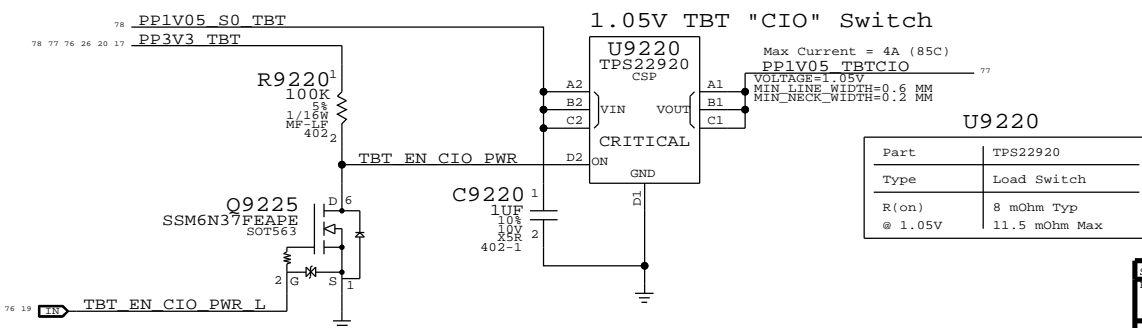


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-3067	1	FRAME,EMI SHIELD,TB	J50 SH9200	CRITICAL?	

TBT "POC" Power-up Reset
Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

Part	TPS22924C
Type	Load Switch
R(on)	20.3 mOhm Typ
@ 1.0V	28.6 mOhm Max

Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ
@ 1.05V	11.5 mOhm Max

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TBT POWER SUPPORT

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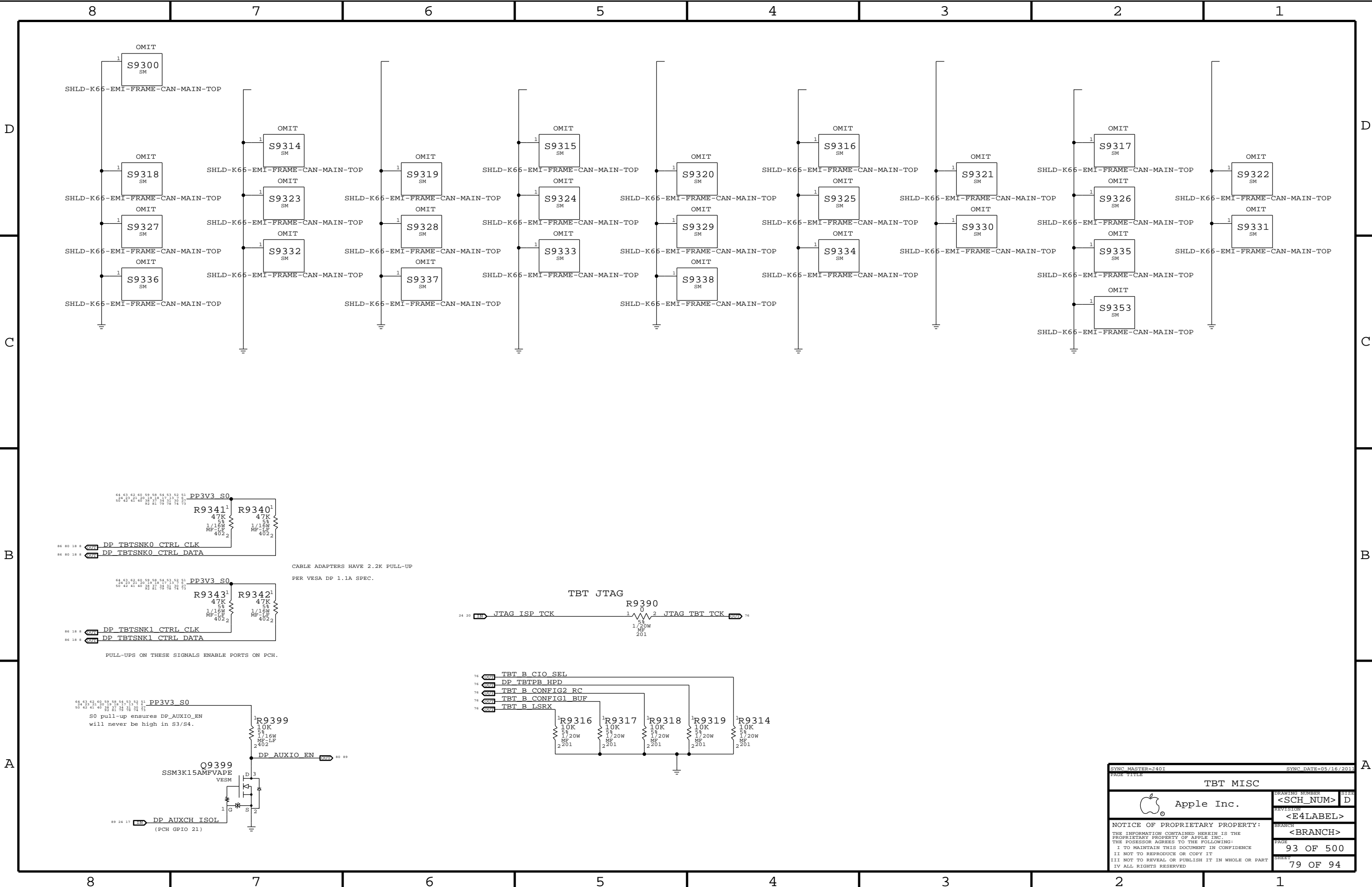
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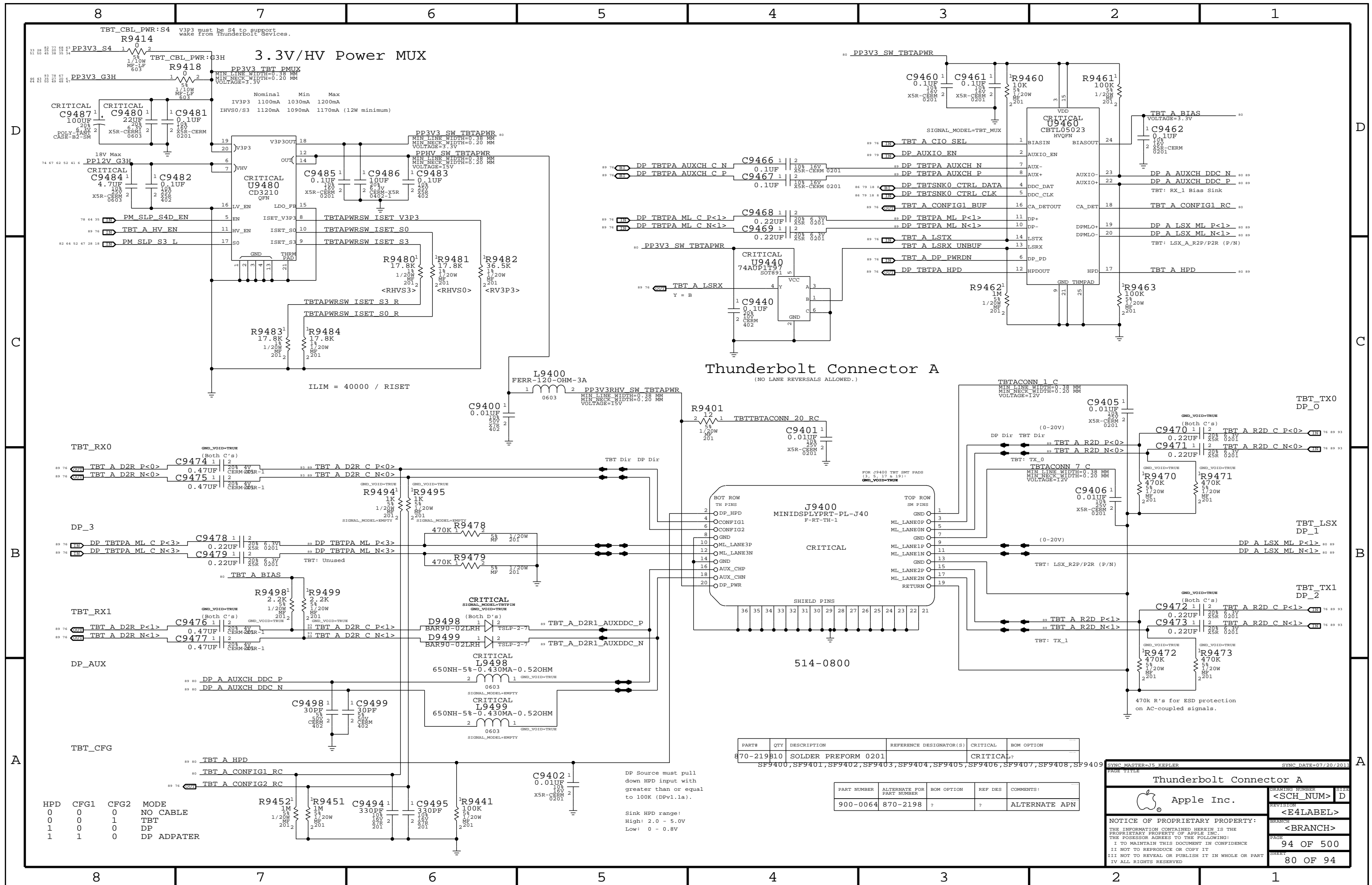
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teknisi-indonesia



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TBT MISC			
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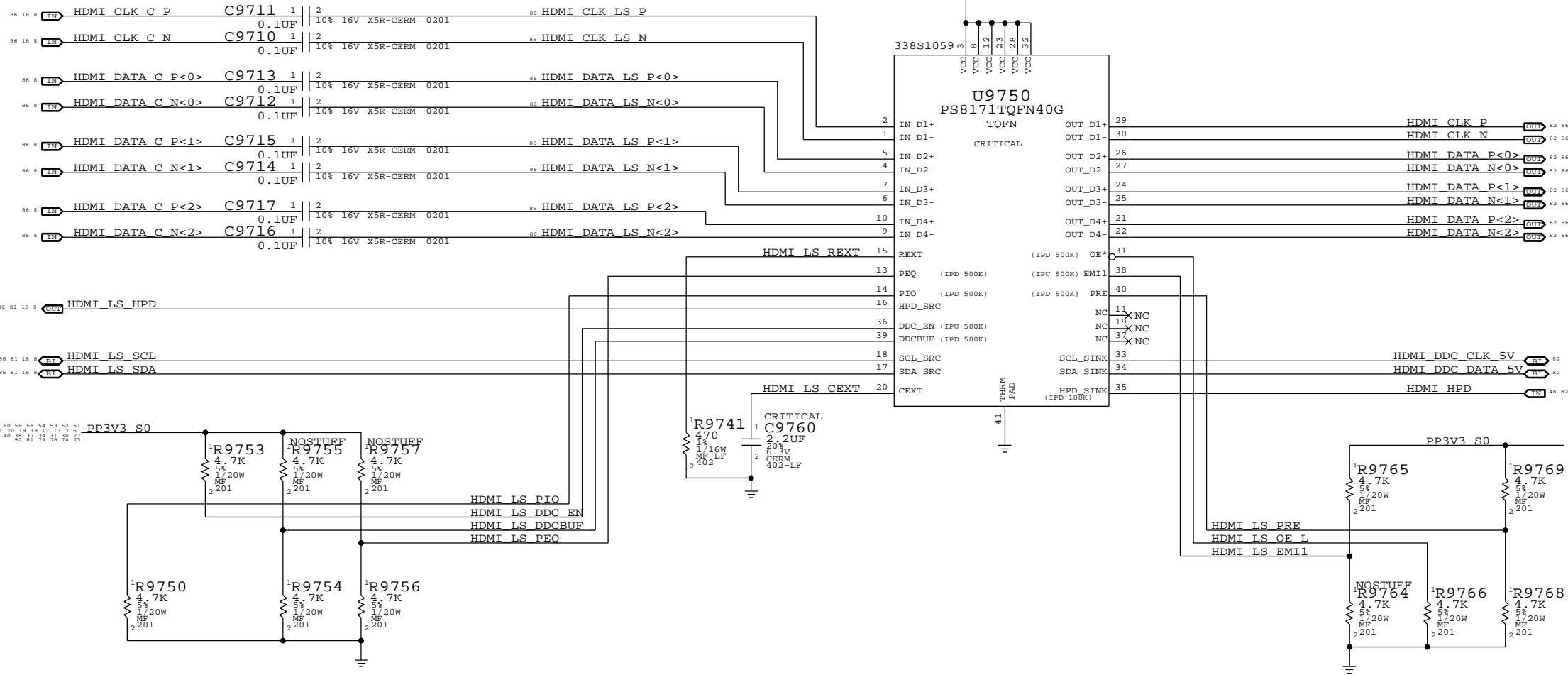
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8 7 6 5 4 3 2 1

ONE 0.1UF AND ONE 0.01UF CAP PER POWER PIN.

PLACE DP CAPS NEXT TO U9750

ALL CHANNELS ARE EQUIVALENT.
LANE SWAPPING AND POLARITY REVERSAL ARE ALLOWED.



AUTO-POWER-DOWN IS ALWAYS ENABLED BU INTERNAL PULL-UP.

PIO - HPD INPUT
HIGH INVERT HPD_SINK
LOW NO INVERSION

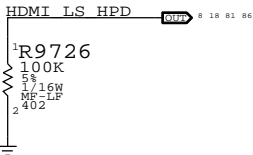
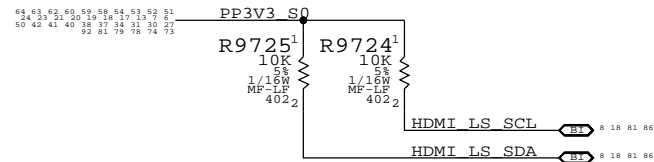
PEQ - INPUT EQ
HIGH HIGH EQ
MID LOW EQ
LOW MID EQ

DDCBUF - DDC LEVEL SHIFTER TYPE
HIGH ACTIVE
LOW PASSIVE


EMI1 - EMI FILTER ENABLE 1
HIGH NO EFFECT
MID (RESERVED)
LOW EMI FILTER ENABLE

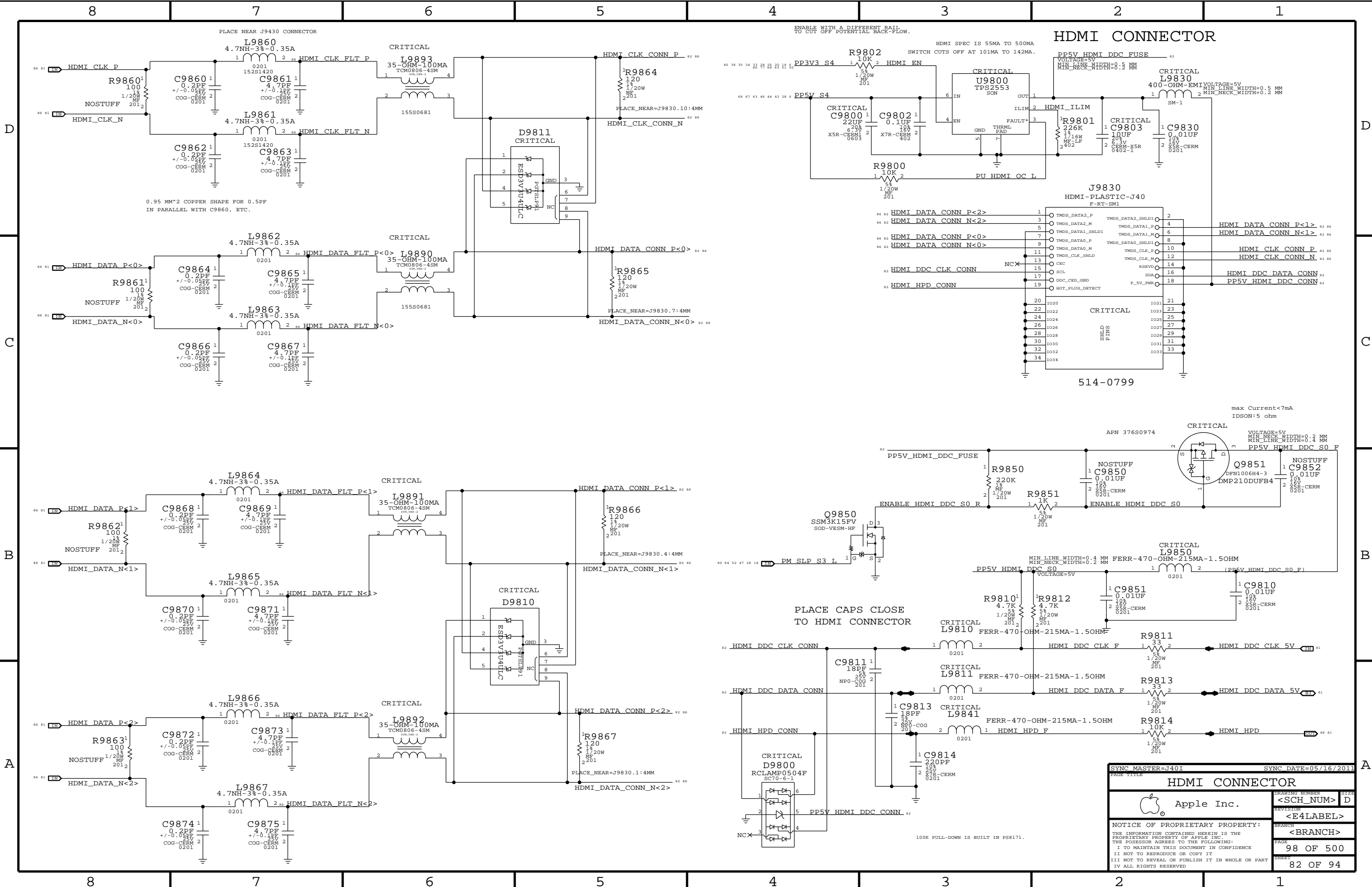
PRE - PRE-EMPHASIS
HIGH LOW PRE-EMPHASIS
MID HIGH PRE-EMPHASIS
LOW NO PRE-EMPHASIS

OE* - OUTPUT ENABLE.
HIGH DISABLE TMD5 DRIVERS
LOW ENABLE TMD5 DRIVERS

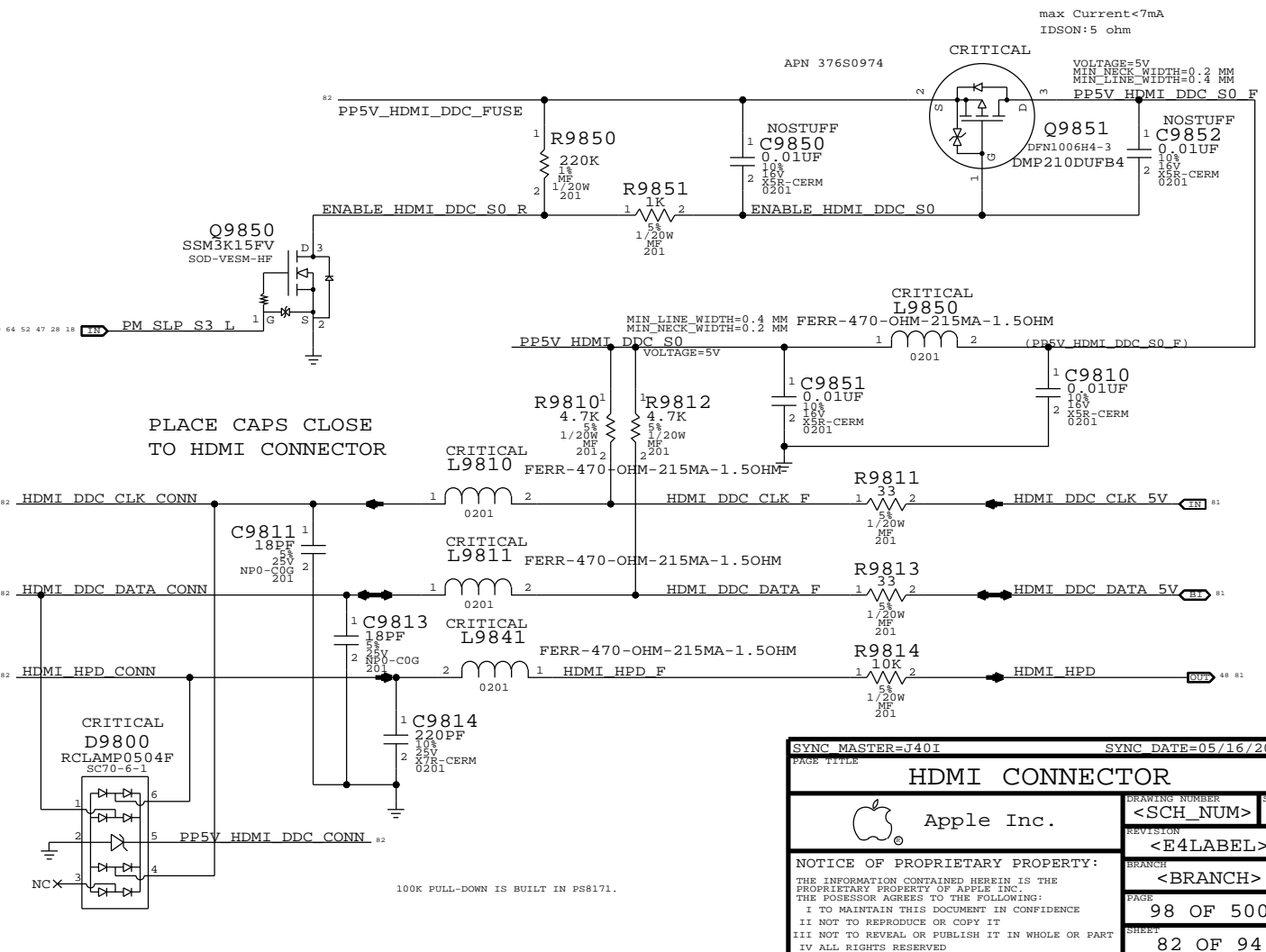
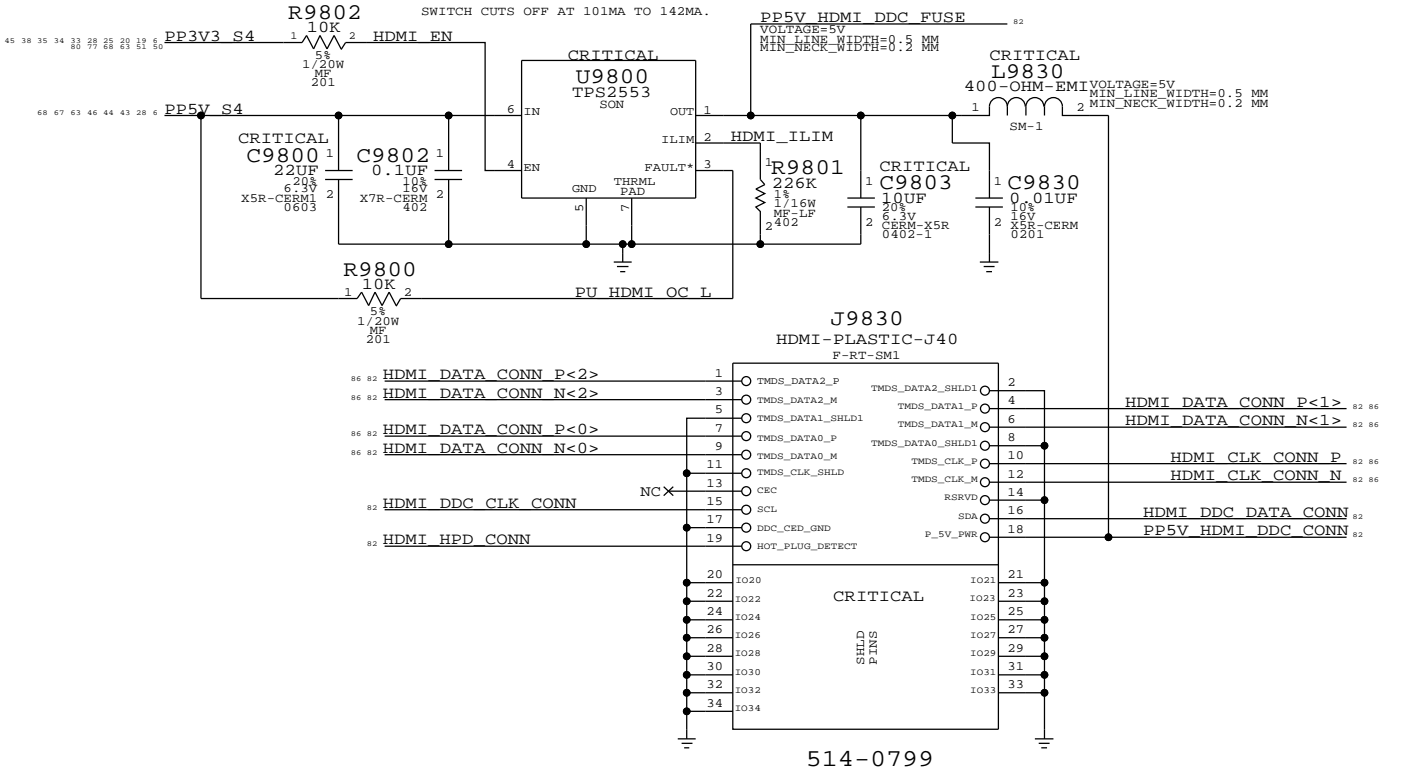



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HDMI SHIFTER			
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HDMI CONNECTOR



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J50* 12 LAYER BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.090 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.090 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.090 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	Y	0.154 MM	0.154 MM	=STANDARD	0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.105 MM	0.105 MM	=STANDARD	0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.110 MM	0.090 MM	=STANDARD	0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.090 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.065 MM	0.065 MM	=STANDARD	0.200 MM	0.200 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_P075	TOP	Y	0.110 MM	0.080 MM	10 MM		
BGA_P075	BOTTOM	Y	0.110 MM	0.073 MM	10 MM		

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

NOTE: Based on K92 m1b stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

Breakout Constraint Overrides

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_QDS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM	MEM_CLK	*	*	MEM_2OTHER
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM	MEM_CTRL	*	*	MEM_2OTHER
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM	MEM_CMD	*	*	MEM_2OTHER
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM	MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM	MEM_DQS	*	*	MEM_2OTHER

DDR3 :

DQ/DM signals should be matched within 0.508mm of associated DQS pair.

DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.

DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].

CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.

CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.















DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.


Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from processor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

SOURCE: HR PDG, Section 4.1.9

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	MEM_A_CLK	85_OHM_DIFF	MEM_CLK	MEM A CLK P<5..0>	12 30
	MEM_A_CLK	85_OHM_DIFF	MEM_CLK	MEM A CLK N<5..0>	12 30
	MEM_A_CNTL	40_OHM_SE	MEM_CTRL	MEM A CKE<3..0>	12 30
	MEM_A_CNTL	40_OHM_SE	MEM_CTRL	MEM A CS L<3..0>	12 30
	MEM_A_CNTL	40_OHM_SE	MEM_CTRL	MEM A ODT<3..0>	12 30
	MEM_A_CMD	40_OHM_SE	MEM_CMD	MEM A A<15..0>	12 30
	MEM_A_CMD	40_OHM_SE	MEM_CMD	MEM A BA<2..0>	12 30
	MEM_A_CMD	40_OHM_SE	MEM_CMD	MEM A CAS L	12 30
	MEM_A_CMD	40_OHM_SE	MEM_CMD	MEM A CAS L	12 30
	MEM_A_CMD	40_OHM_SE	MEM_CMD	MEM A WE L	12 30
	MEM_A_DQ_BYTE0	50_OHM_SE	MEM_DATA	MEM A DQ<7..0>	12 29
	MEM_A_DQ_BYTE1	50_OHM_SE	MEM_DATA	MEM A DQ<15..8>	12 29
	MEM_A_DQ_BYTE2	50_OHM_SE	MEM_DATA	MEM A DQ<23..16>	12 29
	MEM_A_DQ_BYTE3	50_OHM_SE	MEM_DATA	MEM A DQ<31..24>	12 29
	MEM_A_DQ_BYTE4	50_OHM_SE	MEM_DATA	MEM A DQ<39..32>	12 29 30
	MEM_A_DQ_BYTE5	50_OHM_SE	MEM_DATA	MEM A DQ<47..40>	12 29
	MEM_A_DQ_BYTE6	50_OHM_SE	MEM_DATA	MEM A DQ<55..48>	12 29
	MEM_A_DQ_BYTE7	50_OHM_SE	MEM_DATA	MEM A DQ<63..56>	12 29
	MEM_A_DQS0	85_OHM_DIFF	MEM_DQS	MEM A DQS P<0>	12 29
	MEM_A_DQS0	85_OHM_DIFF	MEM_DQS	MEM A DQS N<0>	12 29
	MEM_A_DQS1	85_OHM_DIFF	MEM_DQS	MEM A DQS P<1>	12 29
	MEM_A_DQS1	85_OHM_DIFF	MEM_DQS	MEM A DQS N<1>	12 29
	MEM_A_DQS2	85_OHM_DIFF	MEM_DQS	MEM A DQS P<2>	12 29
	MEM_A_DQS2	85_OHM_DIFF	MEM_DQS	MEM A DQS N<2>	12 29
	MEM_A_DQS3	85_OHM_DIFF	MEM_DQS	MEM A DQS P<3>	12 29
	MEM_A_DQS3	85_OHM_DIFF	MEM_DQS	MEM A DQS N<3>	12 29
	MEM_A_DQS4	85_OHM_DIFF	MEM_DQS	MEM A DQS P<4>	12 29
	MEM_A_DQS4	85_OHM_DIFF	MEM_DQS	MEM A DQS N<4>	12 29
	MEM_A_DQS5	85_OHM_DIFF	MEM_DQS	MEM A DQS P<5>	12 29
	MEM_A_DQS5	85_OHM_DIFF	MEM_DQS	MEM A DQS N<5>	12 29
	MEM_A_DQS6	85_OHM_DIFF	MEM_DQS	MEM A DQS P<6>	12 29 30
	MEM_A_DQS6	85_OHM_DIFF	MEM_DQS	MEM A DQS N<6>	12 29 30
	MEM_A_DQS7	85_OHM_DIFF	MEM_DQS	MEM A DQS P<7>	12 29
	MEM_A_DQS7	85_OHM_DIFF	MEM_DQS	MEM A DQS N<7>	12 29
	MEM_B_CLK	85_OHM_DIFF	MEM_CLK	MEM B CLK P<5..0>	12 31
	MEM_B_CLK	85_OHM_DIFF	MEM_CLK	MEM B CLK N<5..0>	12 31
	MEM_B_CNTL	40_OHM_SE	MEM_CTRL	MEM B CKE<3..0>	12 31
	MEM_B_CNTL	40_OHM_SE	MEM_CTRL	MEM B CS L<3..0>	12 31
	MEM_B_CNTL	40_OHM_SE	MEM_CTRL	MEM B ODT<3..0>	12 31
	MEM_B_CMD	40_OHM_SE	MEM_CMD	MEM B A<15..0>	12 31
	MEM_B_CMD	40_OHM_SE	MEM_CMD	MEM B BA<2..0>	12 31
	MEM_B_CMD	40_OHM_SE	MEM_CMD	MEM B RAS L	12 31
	MEM_B_CMD	40_OHM_SE	MEM_CMD	MEM B CAS L	12 31
	MEM_B_CMD	40_OHM_SE	MEM_CMD	MEM B WE L	12 31
	MEM_B_DQ_BYTE0	50_OHM_SE	MEM_DATA	MEM B DQ<7..0>	12 29
	MEM_B_DQ_BYTE1	50_OHM_SE	MEM_DATA	MEM B DQ<15..8>	12 29
	MEM_B_DQ_BYTE2	50_OHM_SE	MEM_DATA	MEM B DQ<23..16>	12 29
	MEM_B_DQ_BYTE3	50_OHM_SE	MEM_DATA	MEM B DQ<31..24>	12 29
	MEM_B_DQ_BYTE4	50_OHM_SE	MEM_DATA	MEM B DQ<39..32>	12 29 31
	MEM_B_DQ_BYTE5	50_OHM_SE	MEM_DATA	MEM B DQ<47..40>	12 29
	MEM_B_DQ_BYTE6	50_OHM_SE	MEM_DATA	MEM B DQ<55..48>	12 29
	MEM_B_DQ_BYTE7	50_OHM_SE	MEM_DATA	MEM B DQ<63..56>	12 29
	MEM_B_DQS0	85_OHM_DIFF	MEM_DQS	MEM B DQS P<0>	12 29
	MEM_B_DQS0	85_OHM_DIFF	MEM_DQS	MEM B DQS N<0>	12 29
	MEM_B_DQS1	85_OHM_DIFF	MEM_DQS	MEM B DQS P<1>	12 29
	MEM_B_DQS1	85_OHM_DIFF	MEM_DQS	MEM B DQS N<1>	12 29
	MEM_B_DQS2	85_OHM_DIFF	MEM_DQS	MEM B DQS P<2>	12 29
	MEM_B_DQS2	85_OHM_DIFF	MEM_DQS	MEM B DQS N<2>	12 29
	MEM_B_DQS3	85_OHM_DIFF	MEM_DQS	MEM B DQS P<3>	12 29
	MEM_B_DQS3	85_OHM_DIFF	MEM_DQS	MEM B DQS N<3>	12 29
	MEM_B_DQS4	85_OHM_DIFF	MEM_DQS	MEM B DQS P<4>	12 29
	MEM_B_DQS4	85_OHM_DIFF	MEM_DQS	MEM B DQS N<4>	12 29
	MEM_B_DQS5	85_OHM_DIFF	MEM_DQS	MEM B DQS P<5>	12 29
	MEM_B_DQS5	85_OHM_DIFF	MEM_DQS	MEM B DQS N<5>	12 29
	MEM_B_DQS6	85_OHM_DIFF	MEM_DQS	MEM B DQS P<6>	12 29 31
	MEM_B_DQS6	85_OHM_DIFF	MEM_DQS	MEM B DQS N<6>	12 29 31
	MEM_B_DQS7	85_OHM_DIFF	MEM_DQS	MEM B DQS P<7>	12 29
	MEM_B_DQS7	85_OHM_DIFF	MEM_DQS	MEM B DQS N<7>	12 29

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=4:1_SPACING	?
TMDS	*	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP, BOTTOM	=4:1_SPACING	?
TMDS	TOP, BOTTOM	=4:1_SPACING	?

SOURCE: HR PDG, TABLES 191,193, Radeon TRM section 7.7.1
PER ANIL: MODIFIED DP CONNECTOR NEEDS 90 OHMS. MEASURE PROTO BOARD AND ADJUST IF NEEDED.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP, BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 AND 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4:1_SPACING	?
USB3	*	=5:1_SPACING	?
USB_RBIAS	*	15 MIL	?
























SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP, BOTTOM	= 4 : 1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH USB NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
		PHYSICAL	SPACING
USB_HUB_UP	85_OHM_DIFF	USR	USB_HUB_UP_N
USB_HUB_UP_P	85_OHM_DIFF	USR	USB_HUB_UP_P
USB_EXT_A	85_OHM_DIFF	USR	USB_EXT_A_N
USB_EXT_A_P	85_OHM_DIFF	USR	USB_EXT_A_P
USB_EXT_B	85_OHM_DIFF	USR	USB_EXT_B_N
USB_EXT_B_P	85_OHM_DIFF	USR	USB_EXT_B_P
USB_EXT_C	85_OHM_DIFF	USR	USB_EXT_C_N
USB_EXT_C_P	85_OHM_DIFF	USR	USB_EXT_C_P
USB_EXT_D	85_OHM_DIFF	USR	USB_EXT_D_N
USB_EXT_D_P	85_OHM_DIFF	USR	USB_EXT_D_P
USB2_EXT_A_F_N	85_OHM_DIFF	USR	USB2_EXT_A_F_N
USB2_EXT_A_F_P	85_OHM_DIFF	USR	USB2_EXT_A_F_P
USB2_EXT_B_F_N	85_OHM_DIFF	USR	USB2_EXT_B_F_N
USB2_EXT_B_F_P	85_OHM_DIFF	USR	USB2_EXT_B_F_P
USB2_EXT_C_F_N	85_OHM_DIFF	USR	USB2_EXT_C_F_N
USB2_EXT_C_F_P	85_OHM_DIFF	USR	USB2_EXT_C_F_P
USB2_EXT_D_F_N	85_OHM_DIFF	USR	USB2_EXT_D_F_N
USB2_EXT_D_F_P	85_OHM_DIFF	USR	USB2_EXT_D_F_P
USB2_EXT_A_MUXED_N	85_OHM_DIFF	USR	USB2_EXT_A_MUXED_N
USB2_EXT_A_MUXED_P	85_OHM_DIFF	USR	USB2_EXT_A_MUXED_P
USB_EXTB_XHCI_P	85_OHM_DIFF	USR	USB_EXTB_XHCI_P
USB_EXTB_XHCI_N	85_OHM_DIFF	USR	USB_EXTB_XHCI_N
USB_EXTD_XHCI_P	85_OHM_DIFF	USR	USB_EXTD_XHCI_P
USB_EXTD_XHCI_N	85_OHM_DIFF	USR	USB_EXTD_XHCI_N
USB_EXTB_EHCI_P	85_OHM_DIFF	USR	USB_EXTB_EHCI_P
USB_EXTB_EHCI_N	85_OHM_DIFF	USR	USB_EXTB_EHCI_N
USB_EXTD_EHCI_P	85_OHM_DIFF	USR	USB_EXTD_EHCI_P
USB_EXTD_EHCI_N	85_OHM_DIFF	USR	USB_EXTD_EHCI_N
USB_SMC_P	85_OHM_DIFF	USR	USB_SMC_P
USB_SMC_N	85_OHM_DIFF	USR	USB_SMC_N
USB_SMC_SR_P	85_OHM_DIFF	USR	USB_SMC_SR_P
USB_SMC_SR_N	85_OHM_DIFF	USR	USB_SMC_SR_N
USB_IR_N	85_OHM_DIFF	USR	USB_IR_N
USB_IR_P	85_OHM_DIFF	USR	USB_IR_P
USB_IR_R_N	85_OHM_DIFF	USR	USB_IR_R_N
USB_IR_R_P	85_OHM_DIFF	USR	USB_IR_R_P
USB_BT_N	85_OHM_DIFF	USR	USB_BT_N
USB_BT_P	85_OHM_DIFF	USR	USB_BT_P
USB_BT_CONN_N	85_OHM_DIFF	USR	USB_BT_CONN_N
USB_BT_CONN_P	85_OHM_DIFF	USR	USB_BT_CONN_P
USB_BT_SW_N	85_OHM_DIFF	USR	USB_BT_SW_N
USB_BT_SW_P	85_OHM_DIFF	USR	USB_BT_SW_P
USB3_EXT_A_RX_N	85_OHM_DIFF	USR3	USB3_EXT_A_RX_N
USB3_EXT_A_RX_P	85_OHM_DIFF	USR3	USB3_EXT_A_RX_P
USB3_EXTB_RX_N	85_OHM_DIFF	USR3	USB3_EXTB_RX_N
USB3_EXTB_RX_P	85_OHM_DIFF	USR3	USB3_EXTB_RX_P
USB3_EXTC_RX_N	85_OHM_DIFF	USR3	USB3_EXTC_RX_N
USB3_EXTC_RX_P	85_OHM_DIFF	USR3	USB3_EXTC_RX_P
USB3_EXTD_RX_N	85_OHM_DIFF	USR3	USB3_EXTD_RX_N
USB3_EXTD_RX_P	85_OHM_DIFF	USR3	USB3_EXTD_RX_P
USB3_EXT_A_TX_N	85_OHM_DIFF	USR3	USB3_EXT_A_TX_N
USB3_EXT_A_TX_P	85_OHM_DIFF	USR3	USB3_EXT_A_TX_P
USB3_EXTB_TX_N	85_OHM_DIFF	USR3	USB3_EXTB_TX_N
USB3_EXTB_TX_P	85_OHM_DIFF	USR3	USB3_EXTB_TX_P
USB3_EXTC_TX_N	85_OHM_DIFF	USR3	USB3_EXTC_TX_N
USB3_EXTC_TX_P	85_OHM_DIFF	USR3	USB3_EXTC_TX_P
USB3_EXTD_TX_N	85_OHM_DIFF	USR3	USB3_EXTD_TX_N
USB3_EXTD_TX_P	85_OHM_DIFF	USR3	USB3_EXTD_TX_P
USB3_EXT_A_RX_F_N	85_OHM_DIFF	USR3	USB3_EXT_A_RX_F_N
USB3_EXT_A_RX_F_P	85_OHM_DIFF	USR3	USB3_EXT_A_RX_F_P
USB3_EXTB_RX_F_N	85_OHM_DIFF	USR3	USB3_EXTB_RX_F_N
USB3_EXTB_RX_F_P	85_OHM_DIFF	USR3	USB3_EXTB_RX_F_P
USB3_EXTC_RX_F_N	85_OHM_DIFF	USR3	USB3_EXTC_RX_F_N
USB3_EXTC_RX_F_P	85_OHM_DIFF	USR3	USB3_EXTC_RX_F_P
USB3_EXTD_RX_F_N	85_OHM_DIFF	USR3	USB3_EXTD_RX_F_N
USB3_EXTD_RX_F_P	85_OHM_DIFF	USR3	USB3_EXTD_RX_F_P
USB3_EXT_A_TX_F_N	85_OHM_DIFF	USR3	USB3_EXT_A_TX_F_N
USB3_EXT_A_TX_F_P	85_OHM_DIFF	USR3	USB3_EXT_A_TX_F_P
USB3_EXTB_TX_F_N	85_OHM_DIFF	USR3	USB3_EXTB_TX_F_N
USB3_EXTB_TX_F_P	85_OHM_DIFF	USR3	USB3_EXTB_TX_F_P
USB3_EXTC_TX_F_N	85_OHM_DIFF	USR3	USB3_EXTC_TX_F_N
USB3_EXTC_TX_F_P	85_OHM_DIFF	USR3	USB3_EXTC_TX_F_P
USB3_EXTD_TX_F_N	85_OHM_DIFF	USR3	USB3_EXTD_TX_F_N
USB3_EXTD_TX_F_P	85_OHM_DIFF	USR3	USB3_EXTD_TX_F_P
USB3_EXT_A_RX_C_P	85_OHM_DIFF	USR3	USB3_EXT_A_RX_C_P
USB3_EXTB_RX_C_N	85_OHM_DIFF	USR3	USB3_EXTB_RX_C_N
USB3_EXTB_RX_C_P	85_OHM_DIFF	USR3	USB3_EXTB_RX_C_P
USB3_EXTC_RX_C_N	85_OHM_DIFF	USR3	USB3_EXTC_RX_C_N
USB3_EXTC_RX_C_P	85_OHM_DIFF	USR3	USB3_EXTC_RX_C_P
USB3_EXTD_RX_C_N	85_OHM_DIFF	USR3	USB3_EXTD_RX_C_N
USB3_EXTD_RX_C_P	85_OHM_DIFF	USR3	USB3_EXTD_RX_C_P
USB3_EXT_A_TX_C_P	85_OHM_DIFF	USR3	USB3_EXT_A_TX_C_P
USB3_EXTB_TX_C_N	85_OHM_DIFF	USR3	USB3_EXTB_TX_C_N
USB3_EXTB_TX_C_P	85_OHM_DIFF	USR3	USB3_EXTB_TX_C_P
USB3_EXTC_TX_C_N	85_OHM_DIFF	USR3	USB3_EXTC_TX_C_N
USB3_EXTC_TX_C_P	85_OHM_DIFF	USR3	USB3_EXTC_TX_C_P
USB3_EXTD_TX_C_N	85_OHM_DIFF	USR3	USB3_EXTD_TX_C_N
USB3_EXTD_TX_C_P	85_OHM_DIFF	USR3	USB3_EXTD_TX_C_P

DP Properties


ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNKO ML C N<3..0> 8 18 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNKO ML C P<3..0> 8 18 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNKO ML N<3..0> 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNKO ML P<3..0> 76
		55_OHM_SE	DISPLAYPORT	DP TBTSNKO CTRL CLK 8 18 79
		55_OHM_SE	DISPLAYPORT	DP TBTSNKO CTRL DATA 8 18 79
		55_OHM_SE	DISPLAYPORT	DP TBTSNKO HPD 8 18 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNKO AUXCH C N 8 18 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNKO AUXCH C P 8 18 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNKO AUXCH N 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNKO AUXCH P 76
				
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNK1 ML C N<3..0> 8 18 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNK1 ML C P<3..0> 8 18 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNK1 ML N<3..0> 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNK1 ML P<3..0> 76
		55_OHM_SE	DISPLAYPORT	DP TBTSNK1 CTRL CLK 8 18 79
		55_OHM_SE	DISPLAYPORT	DP TBTSNK1 CTRL DATA 8 18 79
		55_OHM_SE	DISPLAYPORT	DP TBTSNK1 HPD 8 18 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNK1 AUXCH C N 8 18 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNK1 AUXCH C P 8 18 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNK1 AUXCH N 76
		85_OHM_DIFF	DISPLAYPORT	DP TBTSNK1 AUXCH P 76

HDMI Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		100_OHM_DIFF	TMDS	HDMI_CLK_CONN_N 0.2
		100_OHM_DIFF	TMDS	HDMI_CLK_CONN_P 0.2
		100_OHM_DIFF	TMDS	HDMI_CLK_FLT_N 0.2
		100_OHM_DIFF	TMDS	HDMI_CLK_FLT_P 0.2
		85_OHM_DIFF	TMDS	HDMI_CLK_C_N 0.18 0.1
		85_OHM_DIFF	TMDS	HDMI_CLK_C_P 0.18 0.1
		85_OHM_DIFF	TMDS	HDMI_CLK_LS_N 0.1
		85_OHM_DIFF	TMDS	HDMI_CLK_LS_P 0.1
		100_OHM_DIFF	TMDS	HDMI_CLK_N 0.1 0.2
		100_OHM_DIFF	TMDS	HDMI_CLK_P 0.1 0.2
		100_OHM_DIFF	TMDS	HDMI_DATA_CONN N<2..0> 0.2
		100_OHM_DIFF	TMDS	HDMI_DATA_CONN P<2..0> 0.2
		100_OHM_DIFF	TMDS	HDMI_DATA_FLT N<2..0> 0.2
		100_OHM_DIFF	TMDS	HDMI_DATA_FLT P<2..0> 0.2
		85_OHM_DIFF	TMDS	HDMI_DATA_C N<2..0> 0.18 0.1
		85_OHM_DIFF	TMDS	HDMI_DATA_C P<2..0> 0.18 0.1
		85_OHM_DIFF	TMDS	HDMI_DATA_LS N<2..0> 0.1
		85_OHM_DIFF	TMDS	HDMI_DATA_LS P<2..0> 0.1
		100_OHM_DIFF	TMDS	HDMI_DATA_N<2..0> 0.1 0.2
		100_OHM_DIFF	TMDS	HDMI_DATA_P<2..0> 0.1 0.2
		55_OHM_SE	TMDS	HDMI_LS_SCL 0.18 0.1
		55_OHM_SE	TMDS	HDMI_LS_SDA 0.18 0.1
		55_OHM_SE	TMDS	HDMI_LS_HPD 0.18 0.1

SATA PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD1 D2R CONN N	42 93
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD1 D2R CONN P	42 93
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD1 D2R N	17 42
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD1 D2R P	17 42
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD1 R2D CONN N	42 93
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD1 R2D CONN P	42 93
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD1 R2D C N	17 42
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD1 R2D C P	17 42
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD2 D2R CONN N	42 93
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD2 D2R CONN P	42 93
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD2 D2R N	17 42
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD2 D2R P	17 42
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD2 R2D CONN N	42 93
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD2 R2D CONN P	42 93
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD2 R2D C N	17 42
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD2 R2D C P	17 42
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD1 D2R DF N	42
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD1 D2R DF P	42
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD1 R2D DF N	42
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD1 R2D DF P	42
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD2 D2R DF N	42
	SATA_HDD_D2R	90_OHM_DIFF	SATA	SATA HDD2 D2R DF P	42
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD2 R2D DF N	42
	SATA_HDD_R2D	90_OHM_DIFF	SATA	SATA HDD2 R2D DF P	42
	PCH_SATA3_ICOMP	50_OHM_SE	SATA_ICOMP	PCH SATA3COMP	17
	PCH_SATA1_ICOMP	17_OHM_SE	SATA_ICOMP	PCH SATA1COMP	17
	PCH_USB_RBIAS		USB_RBIAS	PCH USB RBIAS	19

SYNC MASTER=J40I		SYNC DATE=05/16/2011	
PAGE TITLE			
PCH Constraints 1			
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	= 2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	= 2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL		SPACING			
	LPC_AD	50_OHM_SE	LPC	LPC_AD<3..0>	17	47	49		
		50_OHM_SE	LPC	LPC_AD R<3..0>	17				
	LPC_FRAME_L	50_OHM_SE	LPC	LPC_FRAME_L	17	47	49		
		50_OHM_SE	LPC	LPC_FRAME_R_L	17				
	LPC_RESET_L	50_OHM_SE	LPC	LPCPLUS RESET_L	27	49			
	PCH_LPC_CLK0	50_OHM_SE	CLK_LPC	LPC_CLK33M_SMC_R	19	27			
		50_OHM_SE	CLK_LPC	LPC_CLK33M_SMC	27	47			
		50_OHM_SE	CLK_LPC	LPC_CLK33M_LPCPLUS	27	49			
		50_OHM_SE	CLK_LPC	LPC_CLK33M_LPCPLUS_R	19	27			
	SMB_50S	SMB		SMB_PCH_STR_SCL	50				
		SMB		SMB_PCH_STR_SDA	50				
		SMB		SMB_PCH_DIMM_SCL	30	31	50		
		SMB		SMB_PCH_DIMM_SDA	30	31	50		
		SMB		SMB_PCH_MKY_SCL	50	59	60		
		SMB		SMB_PCH_MKY_SDA	50	59	60		
		SMB		SMB_PCH_VRF_SCL	33	50			
		SMB		SMB_PCH_VRF_SDA	33	50			
	SMBUS_PCH_CLK	SMB		SMBUS_PCH_CLK				DIFFERENTIAL_PAIR	
		SMB		SMBUS_PCH_DATA				SMBUS_PCH	17
		SMB		SMB_PCH_XDP_SCL				SMBUS_PCH_0	17
		SMB		SMB_PCH_XDP_SDA				SMBUS_PCH_0	24
		SMB		SML_PCH_1_CLK	17	50		SMBUS_PCH_0	24
		SMB		SML_PCH_1_DATA	17	50			
	SPT_CLK	55_OHM_SE	SPT	SPI_CLK_R	17	49			
		55_OHM_SE	SPT	SPI_CLK	49	93			
	SPT_MOST	55_OHM_SE	SPT	SPI_MOSI_R	17	49			
		55_OHM_SE	SPT	SPI_MOSI	49	93			
	SPT_MISO	55_OHM_SE	SPT	SPI_MISO	17	49	93		
	SPT_CS0	55_OHM_SE	SPT	SPI_CS0_R_L	17	49			
		55_OHM_SE	SPT	SPI_CS0_L	49	93			
	HDA_BIT_CLK	50_OHM_SE	HDA	HDA_BIT_CLK	17	54			
		50_OHM_SE	HDA	HDA_BIT_CLK_R	17				
	HDA_SYNC	50_OHM_SE	HDA	HDA_SYNC	17	54			
		50_OHM_SE	HDA	HDA_SYNC_R	17				
	HDA_RST_L	50_OHM_SE	HDA	HDA_RST_R_L	17				
		50_OHM_SE	HDA	HDA_RST_L	17	54			
	HDA_SDIN0	50_OHM_SE	HDA	HDA_SDIN0	17	54			
		50_OHM_SE	HDA	AUD_SDI_R	64				
	HDA_SDOUT	50_OHM_SE	HDA	HDA_SDOUT	17	54			
		50_OHM_SE	HDA	HDA_SDOUT_R	17	27			
	90_OHM_DIFF	CLK_PCIE		PCH_CLK96M_DOT_P	17				
		CLK_PCIE		PCH_CLK96M_DOT_N	17				
		CLK_PCIE		PCH_CLK100M_SATA_P	17				
		CLK_PCIE		PCH_CLK100M_SATA_N	17				
		CLK_PCIE		PCH_CLK14P3M_REFCLK	17				
		CLK_PCIE		PCH_CLK33M_PCIIN	17	27			
	50_OHM_SE	PCIE		PCH_PECI	20				
	50_OHM_SE	CPU_ITP		XDP_DA0_USB_EXT_A_OC_L	24				
		CPU_ITP		XDP_DA1_USB_EXT_B_OC_L	24				
		CPU_ITP		XDP_DA2_USB_EXT_C_OC_L	24				
		CPU_ITP		XDP_DA3_USB_EXT_D_OC_L	24				
		CPU_ITP		XDP_DB0_USB_EXT_B_OC_EHCI_L	24				
		CPU_ITP		XDP_DB1_USB_EXT_D_OC_EHCI_L	24				
		CPU_ITP		XDP_DB2_AP_PWR_EN	24				
		CPU_ITP		XDP_DB3_SDCONN_STATE_CHANGE	24				
		CPU_ITP		XDP_PCH_S5_PWRGD	24				
		CPU_ITP		XDP_PCH_PWRBTN_L	24				
	SMB_50S	CPU_ITP		SMB_CPU_XDP_SDA	24	50			
		CPU_ITP		SMB_CPU_XDP_SCL	24	50			
	50_OHM_SE	CPU_ITP		XDP_PCH_TCK	17	24	26	84	
		CPU_ITP		XDP_FC0	24				
		CPU_ITP		XDP_FC1	24				
		CPU_ITP		XDP_DC0_ISOLATE_CPU_MEM_L	24				
		CPU_ITP		XDP_DC1_MXM_GOOD	24				
		CPU_ITP		XDP_DC2_DP_AUXCH_ISOL	24				
		CPU_ITP		XDP_DC3_SATARDVR_EN	24				
		CPU_ITP		XDP_DD0_DP_GPU_TBT_SEL	24				
		CPU_ITP		XDP_DD1_JTAG_ISP_TCK	24				
		CPU_ITP		XDP_DD2_AUD_IPHS_SWITCH_EN	24				
		CPU_ITP		XDP_DD3_ENET_LOW_PWR	24				
	50_OHM_SE	CPU_ITP		XDPPCH_PLTRST_L	24	27			
		CPU_ITP		XDP_DBRESET_L	11	24	27	84	
		CPU_ITP		XDP_PCH_TDO	17	24	26	84	
	50_OHM_SE	CPU_ITP		XDP_PCH_TDI	17	24	26	84	87
		CPU_ITP		XDP_PCH_TDI	17	24	26	84	87
		CPU_ITP		XDP_PCH_TMS	17	24	26	84	

		25_OHM_DIFF	PCIE	PCIE_ENET_R2D_P	17
		25_OHM_DIFF	PCIE	PCIE_ENET_R2D_N	17
	PCIE_ENET_R2D	25_OHM_DIFF	PCIE	PCIE_ENET_R2D_C_P	17 37
		25_OHM_DIFF	PCIE	PCIE_ENET_R2D_C_N	17 37
	PCIE_ENET_D2R	25_OHM_DIFF	PCIE	PCIE_ENET_D2R_P	17 37
		25_OHM_DIFF	PCIE	PCIE_ENET_D2R_N	17 37
		25_OHM_DIFF	PCIE	PCIE_ENET_D2R_C_P	37
		25_OHM_DIFF	PCIE	PCIE_ENET_D2R_C_N	37
		25_OHM_DIFF	PCIE	PCIE_AP_R2D_P	35 93
		25_OHM_DIFF	PCIE	PCIE_AP_R2D_N	35 93
	PCIE_AP_R2D	25_OHM_DIFF	PCIE	PCIE_AP_R2D_C_P	17 35
		25_OHM_DIFF	PCIE	PCIE_AP_R2D_C_N	17 35
	PCIE_AP_D2R	25_OHM_DIFF	PCIE	PCIE_AP_D2R_P	17 35 93
		25_OHM_DIFF	PCIE	PCIE_AP_D2R_N	17 35 93
		25_OHM_DIFF	PCIE	PCIE_FW_R2D_P	39
		25_OHM_DIFF	PCIE	PCIE_FW_R2D_N	39
	PCIE_FW_R2D	25_OHM_DIFF	PCIE	PCIE_FW_R2D_C_P	17 39
		25_OHM_DIFF	PCIE	PCIE_FW_R2D_C_N	17 39
	PCIE_FW_D2R	25_OHM_DIFF	PCIE	PCIE_FW_D2R_P	17 39
		25_OHM_DIFF	PCIE	PCIE_FW_D2R_N	17 39
		25_OHM_DIFF	PCIE	PCIE_FW_D2R_C_P	39
		25_OHM_DIFF	PCIE	PCIE_FW_D2R_C_N	39
995		90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_FCH_P	17
995		90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_FCH_N	17
995	PCIE_CLK100M_T29	90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_TBT_P	17 76
995		90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_TBT_N	17 76
	PCIE_CLK100M	90_OHM_DIFF	CLK_PCIE	NC_PEG_CLK100MP	8 17 93
		90_OHM_DIFF	CLK_PCIE	NC_PEG_CLK100MN	8 17 93
	PCIE_CLK100M_ENET	90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_ENET_P	17 37
		90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_ENET_N	17 37
995	PCIE_CLK100M_AP	90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	35 93
995		90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	35 93
995	PCIE_CLK100M_AP	90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_AP_P	17 35
		90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_AP_N	17 35
995	PCIE_CLK100M_FW	90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
		90_OHM_DIFF	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
995	PCIE_T29_R2D	25_OHM_DIFF	PCIE	PCIE_TBT_R2D_C_P<3..0>	8 10 76
995	PCIE_T29_R2D	25_OHM_DIFF	PCIE	PCIE_TBT_R2D_C_N<3..0>	8 10 76
995	PCIE_T29_R2D	25_OHM_DIFF	PCIE	PCIE_TBT_R2D_P<3..0>	76
995	PCIE_T29_R2D	25_OHM_DIFF	PCIE	PCIE_TBT_R2D_N<3..0>	76
995	PCIE_T29_D2R	25_OHM_DIFF	PCIE	PCIE_TBT_D2R_P<3..0>	8 10 76
995	PCIE_T29_D2R	25_OHM_DIFF	PCIE	PCIE_TBT_D2R_N<3..0>	8 10 76
995	PCIE_T29_D2R	25_OHM_DIFF	PCIE	PCIE_TBT_D2R_C_P<3..0>	76
995	PCIE_T29_D2R	25_OHM_DIFF	PCIE	PCIE_TBT_D2R_C_N<3..0>	76

SYNC_MASTER=J401		SYNC_DATE=05/16/2011	
PAGE TITLE			
PCH Constraints 2			
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ETHERNET CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	= 3 : 1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	*	0.6 MM	?	ENET_HV	*	*	2KV_SPACING
2KV_SPACING	*	0.50 MM	100	ENET_HV	ENET_HV	*	ENET_MDI
2KV_SPACING	TOP,BOTTOM	1.27 MM	100				

NOTE: 2.2kV isolation needed on all primary-side ethernet signals. Min 1.27mm separation from all other copper on the board!

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	= 3 : 1 _SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
		50_OHM_SE	ENET_3X	SYSCCLK CLK25M ENET	26 37
		50_OHM_SE	ENET_3X	TP ENET CLK25M XTAL0	26 37
		50_OHM_SE	ENET_3X	ENET RESET L	27 34
	ENET_MDI	100_OHM_DIFF	ENET_MDI	ENET MDI P<3..0>	36 37
		100_OHM_DIFF	ENET_MDI	ENET MDI N<3..0>	36 37
ENET		100_OHM_DIFF	ENET_HV	ENET MDI TRAN N<3..0>	36
ENET		100_OHM_DIFF	ENET_HV	ENET MDI TRAN P<3..0>	36
ENET		50_OHM_SE	ENET_HV	ENET CENTER TAP<3..0>	36
ENET			ENET_HV	ENET CMODE REF	36

High-voltage isolated
ethernet signals.

SD Interface Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		55 OHM SE	SD INTERFACE	SDCONN CLK 34
		55 OHM SE	SD INTERFACE	SDCONN CLK FF 34
		55 OHM SE	SD INTERFACE	SDCONN CMD 34
		55 OHM SE	SD INTERFACE	SDCONN CLK <7..0> 34
		55 OHM SE	SD INTERFACE	SDCONN CLK R 34
		55 OHM SE	SD INTERFACE	SDCONN CMD R 34
		55 OHM SE	SD INTERFACE	SDCONN DATA R<7..0> 34
		55 OHM SE	SD INTERFACE	ENET_CR_CLK 37
		55 OHM SE	SD INTERFACE	ENET_CR_CMD 37
		55 OHM SE	SD INTERFACE	ENET_CR DATA<7..0> 37
		55 OHM SE	SD INTERFACE	SDCONN_F CLK 34
		55 OHM SE	SD INTERFACE	SDCONN_F CLK FF 34

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
MIN		110_OHM_DIFF	FW_TP	FW PORT0 TPAL N	
MIN		110_OHM_DIFF	FW_TP	FW PORT0 TPAL P	
MIN		110_OHM_DIFF	FW_TP	FW PORT1 TPA N	39 41
MIN	FW_P1_TPA	110_OHM_DIFF	FW_TP	FW PORT1 TPA P	39 41
MIN		110_OHM_DIFF	FW_TP	FW PORT0 TPBL N	
MIN		110_OHM_DIFF	FW_TP	FW PORT0 TPBL P	
MIN		110_OHM_DIFF	FW_TP	FW PORT1 TPB N	39 41
MIN	FW_P1_TPB	110_OHM_DIFF	FW_TP	FW PORT1 TPB P	39 41
MIN		50_OHM_SE	CLK_PCIE	FW CLK24P576M XI	39
MIN		50_OHM_SE	CLK_PCIE	FW CLK24P576M XO	39
MIN		50_OHM_SE	CLK_PCIE	FW CLK24P576M XO R	39

Port 0 and 2 Not Used

DISPLAYPORT SIGNAL CONSTRAINTS

NOTE: DISPLAYPORT PHYSICAL/SPACING CONSTRAINTS PROVIDED BY CHIPSET OR GPU PAGE.

TBT I2C SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2X_DIELECTRIC	?

TBT SPI SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2X_DIELECTRIC	?


















TBT/DP CONNECTOR SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5X_DIELECTRIC	?	TBTDP	TOP,BOTTOM	=7X_DIELECTRIC	?

SOURCE: BILL CORNELIUS'S TBT ROUTING NOTES

TBT IC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	SMR_50S	TBT_I2C	I2C TBTBTR SCL	50 76
	SMR_50S	TBT_I2C	I2C TBTBTR SDA	50 76
 TBT_SPI_CLK	55_OHM_SE	TBT_SPI	TBT SPI CLK	76
 TBT_SPI_MOSI	55_OHM_SE	TBT_SPI	TBT SPI MOSI	76
 TBT_SPI_MISO	55_OHM_SE	TBT_SPI	TBT SPI MISO	76
 TBT_SPI_CS_L	55_OHM_SE	TBT_SPI	TBT SPI CS_L	76
		TBT_I2C	TBT A LSTX	76 80
		TBT_I2C	TBT A LSRX	76 80
		TBT_I2C	TBT A CONFIG1 BUF	76 80
		TBT_I2C	TBT A CONFIG2 RC	76 80
		TBT_I2C	TBT A HV EN	76 80
		TBT_I2C	TBT A CIO SEL	76 80
		TBT_I2C	TBT A DP PWRDN	76 80
		TBT_I2C	DP TBTPA HPD	76 80
		TBT_I2C	TBT A HPD	80
		TBT_I2C	DP AUXIO EN	79 80
		TBT_I2C	DP AUXCH ISOL	17 24 79

TBT/DP NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
TBT_R2D0	85_OHM_DIFF	TBTDP	TBT A R2D P<0>	80
TBT_R2D0	85_OHM_DIFF	TBTDP	TBT A R2D N<0>	80
TBT_R2D1	85_OHM_DIFF	TBTDP	TBT A R2D P<1>	80
TBT_R2D1	85_OHM_DIFF	TBTDP	TBT A R2D N<1>	80
TBT_D2R0	85_OHM_DIFF	TBTDP	TBT A D2R P<0>	76 80
TBT_D2R0	85_OHM_DIFF	TBTDP	TBT A D2R N<0>	76 80
TBT_D2R1	85_OHM_DIFF	TBTDP	TBT A D2R P<1>	76 80
TBT_D2R1	85_OHM_DIFF	TBTDP	TBT A D2R N<1>	76 80
	85_OHM_DIFF	TBTDP	TBT A R2D C P<1..0>	76 80 93
	85_OHM_DIFF	TBTDP	TBT A R2D C N<1..0>	76 80 93
	85_OHM_DIFF	TBTDP	TBT A D2R C P<1..0>	80 93
	85_OHM_DIFF	TBTDP	TBT A D2R C N<1..0>	80 93
DP	85_OHM_DIFF	TBTDP	TBT A D2R1 AUXDDC P	80
DP	85_OHM_DIFF	TBTDP	TBT A D2R1 AUXDDC N	80
	85_OHM_DIFF	TBTDP	DP A AUXCH DDC P	80
	85_OHM_DIFF	TBTDP	DP A AUXCH DDC N	80
	85_OHM_DIFF	DISPLAYPORT	DP A LSX ML P<1>	80
	85_OHM_DIFF	DISPLAYPORT	DP A LSX ML N<1>	80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA AUXCH P	80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA AUXCH N	80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA AUXCH C P	76 80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA AUXCH C N	76 80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA ML P<3>	80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA ML N<3>	80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA ML C P<3>	76 80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA ML C N<3>	76 80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA ML P<1>	80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA ML N<1>	80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA ML C P<1>	76 80
	85_OHM_DIFF	DISPLAYPORT	DP TBTPA ML C N<1>	76 80

GDDR5 Frame Buffer Signal Constraints







PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE	SET_NAME
	FB_B0_CLK	80_OHM_DIFF	GDDR5_CLK
	FB_B0_CLK	80_OHM_DIFF	GDDR5_CLK
	FB_B1_CLK	80_OHM_DIFF	GDDR5_CLK
	FB_B1_CLK	80_OHM_DIFF	GDDR5_CLK
	FB_B0_CMD	45_OHM_SE	GDDR5_CMD
	FB_B1_CMD	45_OHM_SE	GDDR5_CMD
	FB_B0_CMD	45_OHM_SE	GDDR5_CMD
	FB_B1_CMD	45_OHM_SE	GDDR5_CMD
	FB_B0_CMD	45_OHM_SE	GDDR5_CMD
	FB_B1_CMD	45_OHM_SE	GDDR5_CMD
	FB_B0_CMD	45_OHM_SE	GDDR5_CMD
	FB_B1_CMD	45_OHM_SE	GDDR5_CMD
	FB_B0_CMD_R	45_OHM_SE	GDDR5_CMD
	FB_B1_CMD_R	45_OHM_SE	GDDR5_CMD
	FB_B0_CMD	45_OHM_SE	GDDR5_CMD
	FB_B1_CMD	45_OHM_SE	GDDR5_CMD
	FB_B0_EDC0	45_OHM_SE	GDDR5_EDC
	FB_B0_EDC1	45_OHM_SE	GDDR5_EDC
	FB_B0_EDC2	45_OHM_SE	GDDR5_EDC
	FB_B0_EDC3	45_OHM_SE	GDDR5_EDC
	FB_B1_EDC0	45_OHM_SE	GDDR5_EDC
	FB_B1_EDC1	45_OHM_SE	GDDR5_EDC
	FB_B1_EDC2	45_OHM_SE	GDDR5_EDC
	FB_B1_EDC3	45_OHM_SE	GDDR5_EDC
	FB_B0_DBI_L0	45_OHM_SE	GDDR5_DATA
	FB_B0_DBI_L1	45_OHM_SE	GDDR5_DATA
	FB_B0_DBI_L2	45_OHM_SE	GDDR5_DATA
	FB_B0_DBI_L3	45_OHM_SE	GDDR5_DATA
	FB_B1_DBI_L0	45_OHM_SE	GDDR5_DATA
	FB_B1_DBI_L1	45_OHM_SE	GDDR5_DATA
	FB_B1_DBI_L2	45_OHM_SE	GDDR5_DATA
	FB_B1_DBI_L3	45_OHM_SE	GDDR5_DATA
	FB_B0_WCLK0	80_OHM_DIFF	GDDR5_CMD
	FB_B0_WCLK0	80_OHM_DIFF	GDDR5_CMD
	FB_B0_WCLK1	80_OHM_DIFF	GDDR5_CMD
	FB_B0_WCLK1	80_OHM_DIFF	GDDR5_CMD
	FB_B1_WCLK0	80_OHM_DIFF	GDDR5_CMD
	FB_B1_WCLK0	80_OHM_DIFF	GDDR5_CMD
	FB_B1_WCLK1	80_OHM_DIFF	GDDR5_CMD
	FB_B1_WCLK1	80_OHM_DIFF	GDDR5_CMD
	FB_B0_DQ_BYTE0	45_OHM_SE	GDDR5_DATA
	FB_B0_DQ_BYTE1	45_OHM_SE	GDDR5_DATA
	FB_B0_DQ_BYTE2	45_OHM_SE	GDDR5_DATA
	FB_B0_DQ_BYTE3	45_OHM_SE	GDDR5_DATA
	FB_B1_DQ_BYTE0	45_OHM_SE	GDDR5_DATA
	FB_B1_DQ_BYTE1	45_OHM_SE	GDDR5_DATA
	FB_B1_DQ_BYTE2	45_OHM_SE	GDDR5_DATA
	FB_B1_DQ_BYTE3	45_OHM_SE	GDDR5_DATA
	FB_B0_CMD_R	45_OHM_SE	GDDR5_CMD
	FB_B1_CMD_R	45_OHM_SE	GDDR5_CMD
	</		

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET		DESCRIPTION	VALUE	DESCRIPTION
	GPU_CLK27M	55_OHM_SE	CLK_SLOW	GPU_OSC_27M_XTALIN
	GPU_CLK27M	55_OHM_SE	CLK_SLOW	GPU_OSC_27M_XTALOUT
	GPU_CLK27M	55_OHM_SE	CLK_SLOW	GPU_OSC_27M_XTAL_BUFFOUT
	GPU_CLK27M	55_OHM_SE	CLK_SLOW	GPU_OSC_27M_SSIN
		1:1_DIFFEAIR		PEX_TSTCLK_O_P
		1:1_DIFFEAIR		PEX_TSTCLK_O_N

SYNC MASTER=J40I		SYNC DATE=05/16/2011	
PAGE TITLE		PAGE NUMBER	
GPU (KEPLAR) CONSTRAINTS			
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	= 2 : 1_SPACING	?
THERM	*	= 2 : 1_SPACING	?
AUDIO	*	= 2 : 1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	= STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM




NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
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J50* SPECIFIC NET PROPERTIES

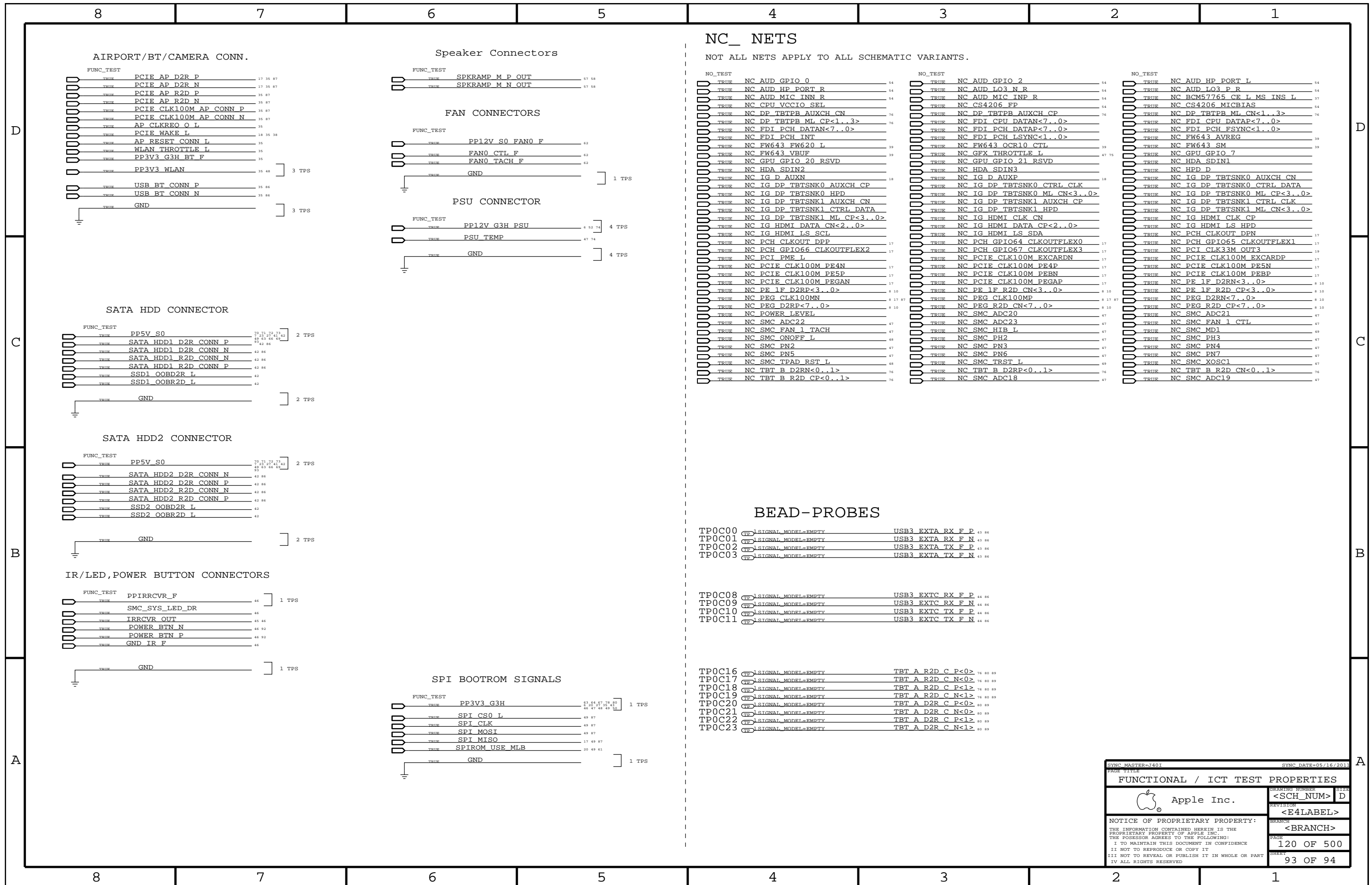
ELECTRICAL_CONSTRAINT_SET		NET_TYPE		SPACING	
		PHYSICAL			
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_VDDQ_P	51
		SENSE_1T01_55S	SENSE	ISNS_VDDQ_N	51
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_P1V05PCH_P	51
		SENSE_1T01_55S	SENSE	ISNS_P1V05PCH_N	51
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	PIV5S3_CS_P	51 68
		SENSE_1T01_55S	SENSE	PIV5S3_CS_N	51 68
	SENSE_DIFFPAIR	VRSENSE	SENSE	CPUVCCIOS0_CS_P	51 72
		VRSENSE	SENSE	CPUVCCIOS0_CS_N	51 72
		VRSENSE	SENSE	CPUVCCIOS0_VO	72
		VRSENSE	SENSE	CPUVCCIOS0_OCSET	72
	SENSE_DIFFPAIR	VRSENSE	SENSE	VCCSA0_CS_P	51 66
		VRSENSE	SENSE	VCCSA0_CS_N	51 66
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_P12VG3H_P	52
		SENSE_1T01_55S	SENSE	ISNS_P12VG3H_N	52
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_CPUDDR_P	52
		SENSE_1T01_55S	SENSE	ISNS_HS_CPUDDR_N	52
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_WLAN_P	35 52
		SENSE_1T01_55S	SENSE	ISNS_WLAN_N	35 52
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_GPU_P	35 52
		SENSE_1T01_55S	SENSE	ISNS_HS_GPU_N	
		50_OHM_SE		AUD_HPAMP_INL_N	56
		50_OHM_SE		AUD_HPAMP_INL_P	56
		50_OHM_SE		AUD_HPAMP_INR_N	56
		50_OHM_SE		AUD_HPAMP_INR_P	56
		50_OHM_SE		EXT_MIC_N	59 60
		50_OHM_SE		EXT_MIC_P	59 60
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LQ3_L_P	54 57
		AUDIODIFF	AUDIO	AUD_LQ3_L_N	54 57
		AUDIODIFF	AUDIO	AUD_SPKRAMP_IN_L_P	57
		AUDIODIFF	AUDIO	AUD_SPKRAMP_IN_L_N	57
		AUDIODIFF	AUDIO	AUD_SPKRAMP_IN_P	57
		AUDIODIFF	AUDIO	AUD_SPKRAMP_IN_N	57
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	AMBIENT_THRMD_N	53
		THERM_1T01_55S	THERM	AMBIENT_THRMD_P	53
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	CPU_PROX_THRM_N	53
		THERM_1T01_55S	THERM	CPU_PROX_THRM_P	53
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	DIMM_PROX_THRM_N	53
		THERM_1T01_55S	THERM	DIMM_PROX_THRM_P	53
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	WIFI_PROX_THRM_N	53
		THERM_1T01_55S	THERM	WIFI_PROX_THRM_P	53
	SENSE_DIFFPAIR	DIFFPAIR		ISNS_TBT1V05_N	78
		DIFFPAIR		ISNS_TBT1V05_P	78
	SENSE_DIFFPAIR	DIFFPAIR		ISNS_TBT3V3_N	78
		DIFFPAIR		ISNS_TBT3V3_P	78
	SENSE_DIFFPAIR	DIFFPAIR		CPU_VDDO_SENSE_N	
		DIFFPAIR		CPU_VDDO_SENSE_P	
		50_OHM_SE		VR_CPU_VSNS_XW_N	
		50_OHM_SE		VR_CPU_VSNS_XW_P	
		50_OHM_SE		VR_AXG_VSNS_XW_N	
		50_OHM_SE		VR_AXG_VSNS_XW_P	
		50_OHM_SE		POWER_BTN_N	46 93
		50_OHM_SE		POWER_BTN_P	46 93
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GFXCORE_N	
		SENSE_1T01_55S	SENSE	GFXCORE_P	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GFXIMVP6_CS_R_P	
		SENSE_1T01_55S	SENSE	GFXIMVP6_CS_R_N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GFXIMVP6_CS_P	
		SENSE_1T01_55S	SENSE	GFXIMVP6_CS_N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GPU_FBVDDO_SENSE_P	
		SENSE_1T01_55S	SENSE	GPU_FBVDDO_SENSE_N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GPUFB_CS_P	
		SENSE_1T01_55S	SENSE	GPUFB_CS_N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GPUVCORE_SENSE_P	
		SENSE_1T01_55S	SENSE	GPUVCORE_SENSE_N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V05_GPU_CS_P	
		SENSE_1T01_55S	SENSE	P1V05_GPU_CS_N	
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V05_GPU_PEX_IOVDD_SNS_P	
		SENSE_1T01_55S	SENSE	P1V05_GPU_PEX_IOVDD_SNS_N	
	SENSE_DIFFPAIR	VRSENSE	SENSE	CPUIMVP_ISNS1_N	51 68
		VRSENSE	SENSE	CPUIMVP_ISNS1_P	51 68
	SENSE_DIFFPAIR	VRSENSE	SENSE	CPUIMVP_ISNS2_N	51 70
		VRSENSE	SENSE	CPUIMVP_ISNS2_P	51 68
	SENSE_DIFFPAIR	VRSENSE	SENSE	CPUIMVP_ISNS3_N	51 70
		VRSENSE	SENSE	CPUIMVP_ISNS3_P	51 68
	SENSE_DIFFPAIR	VRSENSE	SENSE	CPUIMVP_ISNS1G_N	51 71
		VRSENSE	SENSE	CPUIMVP_ISNS1G_P	51 71
	SENSE_DIFFPAIR	VRSENSE	SENSE	CPUIMVP_ISNS2G_N	51 71
		VRSENSE	SENSE	CPUIMVP_ISNS2G_P	

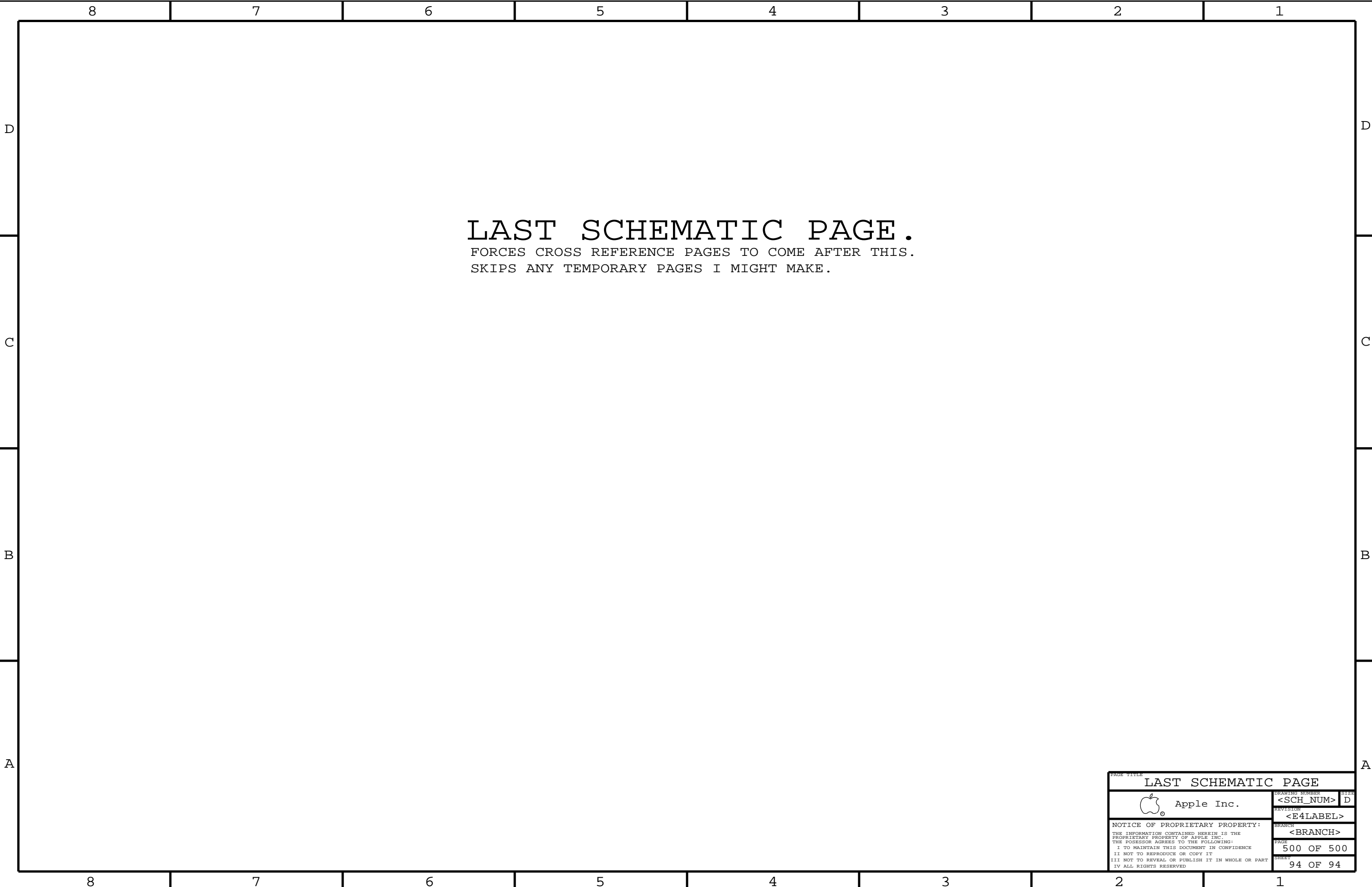
J50* SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
	SB_POWER	PP3V3 S5 6 17 18 19 20 21 23 24 27 28 61 63 64 73
	SB_POWER	PP3V3 S0 52 53 54 58 59 60 62 63 64 73 6 7 13 17 18 19 20 21 23 24 27 30 31 34 37 38 40 41 42 50 51 74 78 79 81
	GND	GND

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
□	SENSE_DIEFFPAIR	THERM_1T01_55S	THERM	CPU THERMD P 10 53
□		THERM_1T01_55S	THERM	CPU THERMD N 10 53
□	SENSE_DIEFFPAIR	THERM_1T01_55S	THERM	GPUTHMSNS D P
□		THERM_1T01_55S	THERM	GPUTHMSNS D N
□	SENSE_DIEFFPAIR	THERM_1T01_55S	THERM	GPU TDIODE P
□		THERM_1T01_55S	THERM	GPU TDIODE N
□				
□	SENSE_DIEFFPAIR	THERM_1T01_55S	THERM	CPU PROX THERM P
□		THERM_1T01_55S	THERM	CPU PROX THERM N
□	SENSE_DIEFFPAIR	THERM_1T01_55S	THERM	WIFI PROX THERM P
□		THERM_1T01_55S	THERM	WIFI PROX THERM N
□	SENSE_DIEFFPAIR	THERM_1T01_55S	THERM	DIMM PROX THERM P
□		THERM_1T01_55S	THERM	DIMM PROX THERM N
□	SENSE_DIEFFPAIR	THERM_1T01_55S	THERM	PCH THRMD P 53
□		THERM_1T01_55S	THERM	PCH THRMD N 53
□	SENSE_DIEFFPAIR	THERM_1T01_55S	THERM	SMT THRM SNS3 P 53
□		THERM_1T01_55S	THERM	SMT THRM SNS3 N 53
□	SENSE_DIEFFPAIR	THERM_1T01_55S	THERM	TBT THRM SNS3 P
□		THERM_1T01_55S	THERM	TBT THRM SNS3 N

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